# PCB Number: 13048-1


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| 50 | GPU_JET IO | |
| 51 | GPU_JET MEMORY | |
| 52 | GPU_JET STRAP | |
| 53 | GPU_JET POWER | |
| 54 | GPU_DDR3 64MX16 | |
| 55 | GPU_POWER CORE | |
| 56 | GPU_POWER 0D95V/1D8V | |
| 57 | GPU_POWER 3D3V/ 1D5V | |


**Model : Tigris AIO**
**PCB version : 1**
**PCB Number: 13048**
**SCH Ver : A00**
**PCBA : A00**

BOM Configuration
(R):Unmount
(G):GPU
(U):UMA
(T):Touch
(E):External Adapter(19V)
(I):Internal PSU(12V)
(S):Tigris AIO
(C):Caspian

***PCB BOARD SIZE***
***6 Layers***
***265mm X 190mm***

**Haswell Platform :**

**LGA1155 : Haswell CPU**

**Chipset : Haswell PCH H81**

<Variant Name>

wistron


Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

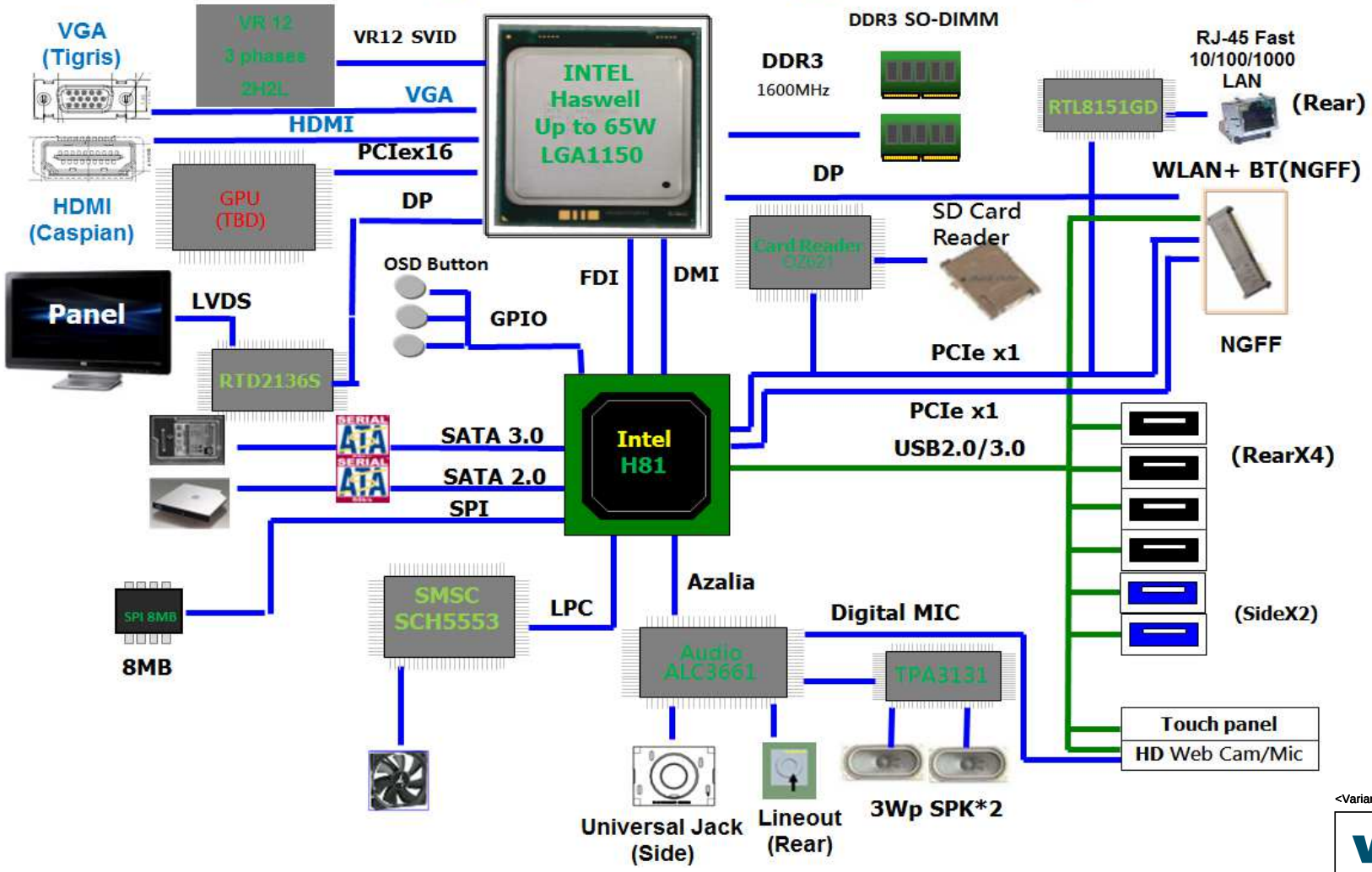

Title: Cover Page

Document Number: Rosa_Tigris AIO

Rev: 1

Monday, January 06, 2014

# Block Diagram for Tigris/Caspian AIO




*PCB BOARD SIZE*
*265mm X 184mm*
*4 Layer*

- *Internal Slot/Header*
- *Front/Rear IO*
- *Chipset*

<Variant Name>

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| | | | |
|---|---|---|---|
| Title | Block Diagram | | |
| Size | Document Number<br>CustomRosa_Tigris AIO | | Rev<br>1 |
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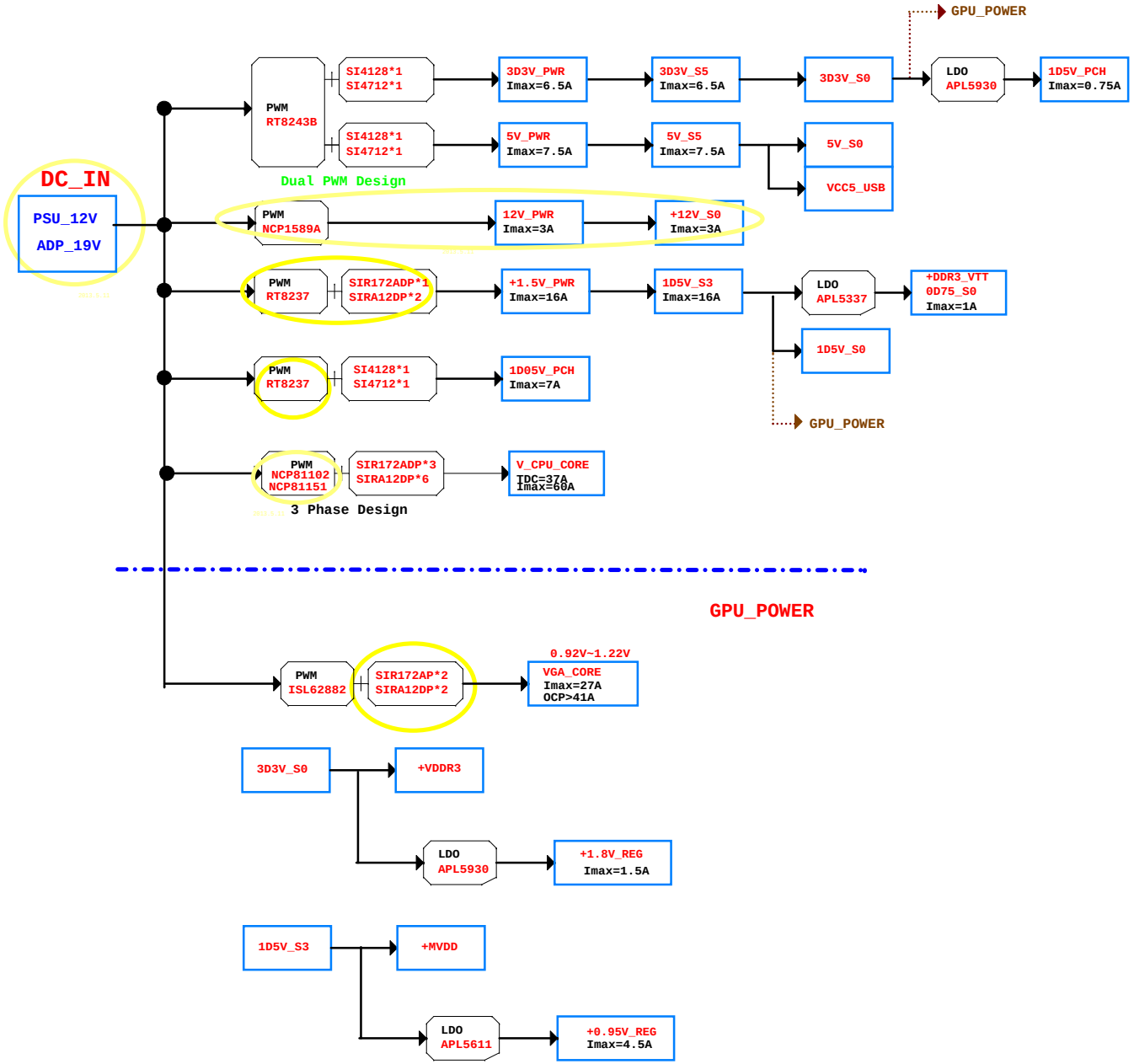


<Variant Name>

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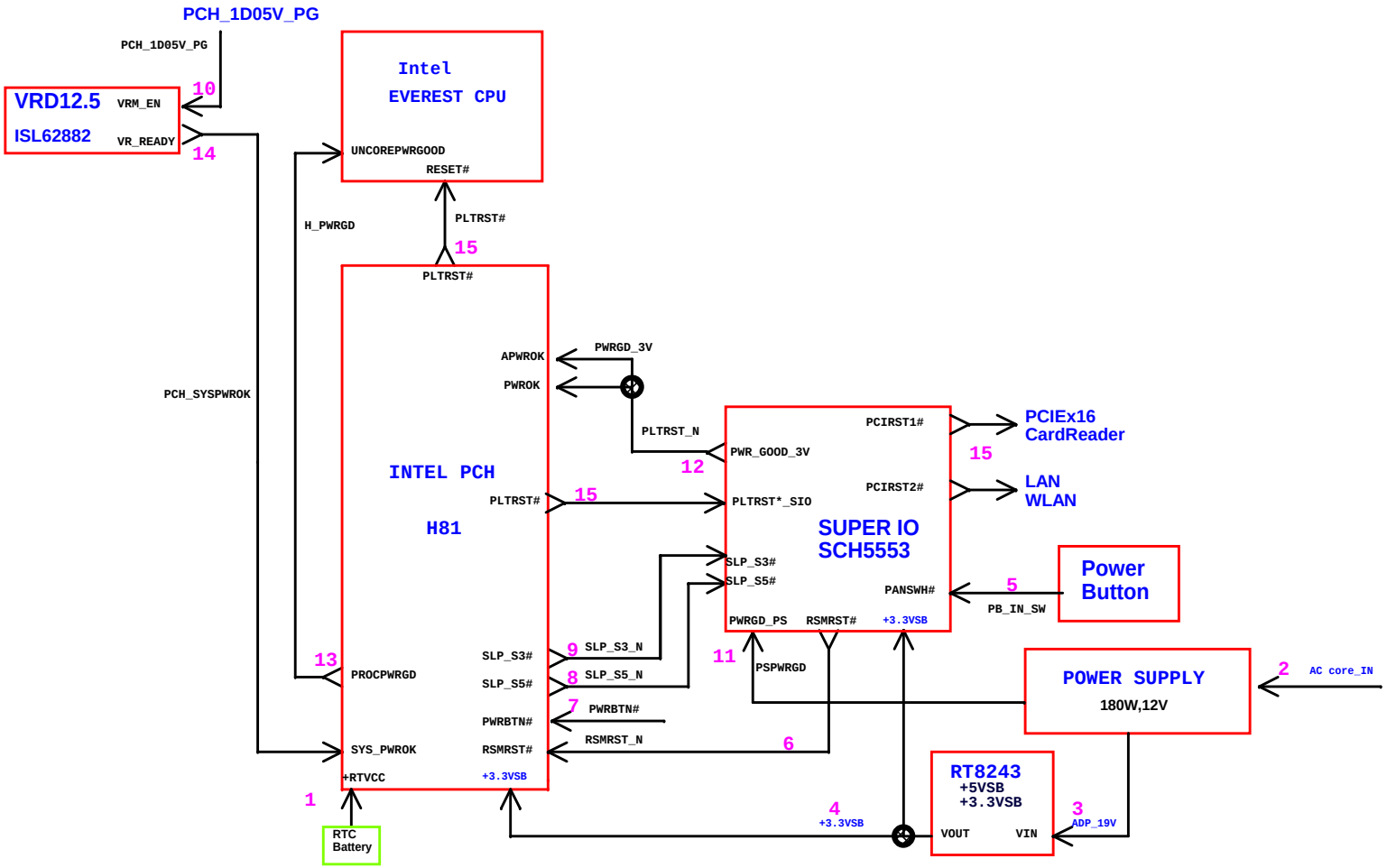
Title: Power Delivery

Rev 1

06, 2014 Sheet 3 of 58




<Variant Name>

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Title: Power Good & Reset Diagram

| Size | Document Number | Rev |
|---|---|---|
| C | Rosa_Tigris AIO | 1 |

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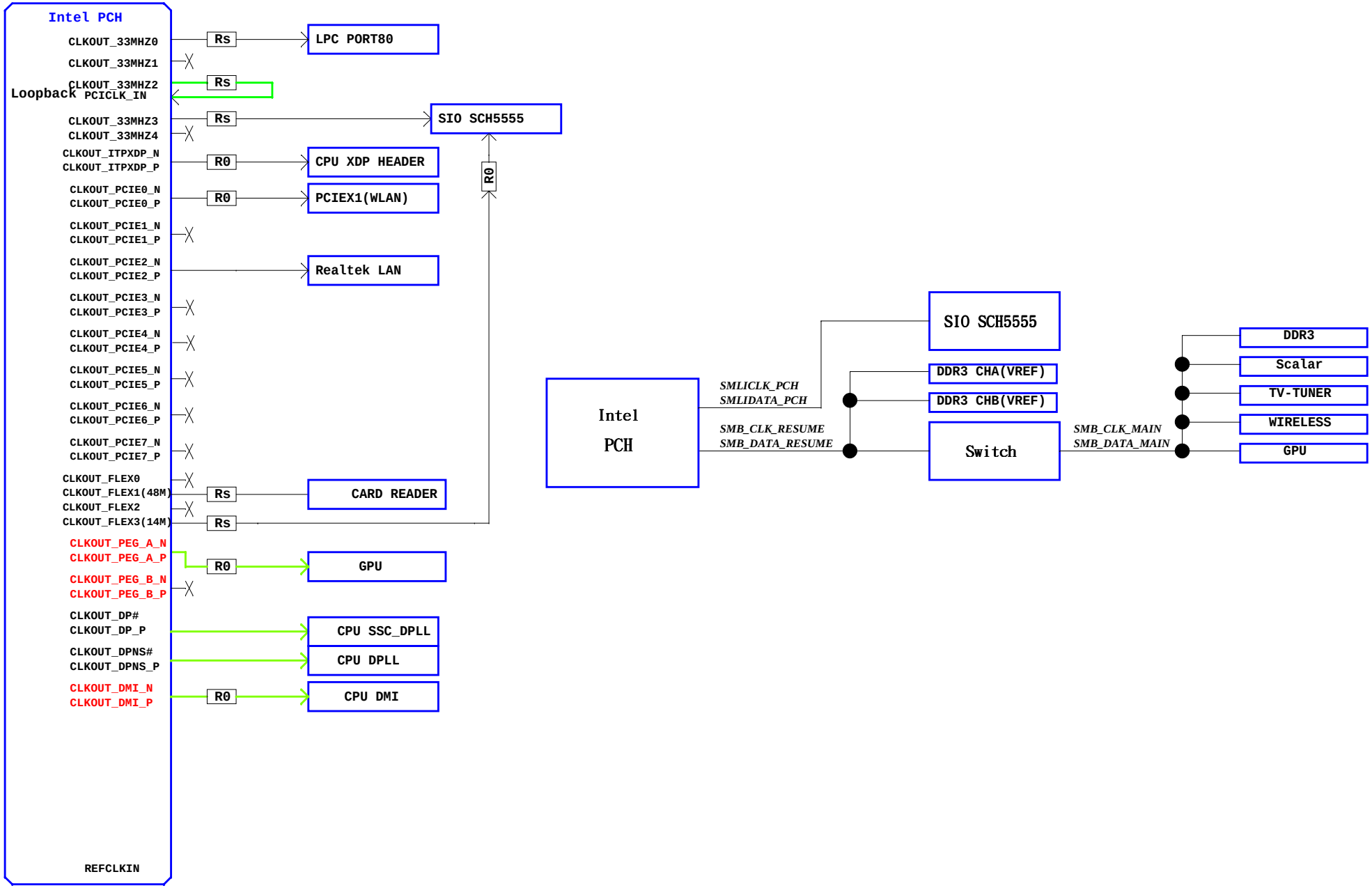


Note: R0 is 0 ohm optional resister
Note: Rs is serie resister
Note: Green Color is direct-parallel option

<Variant Name>

wistron

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Title: Clock Diagram

| Size | Document Number | Rev |
|---|---|---|
| C | Rosa_Tigris AIO | 1 |

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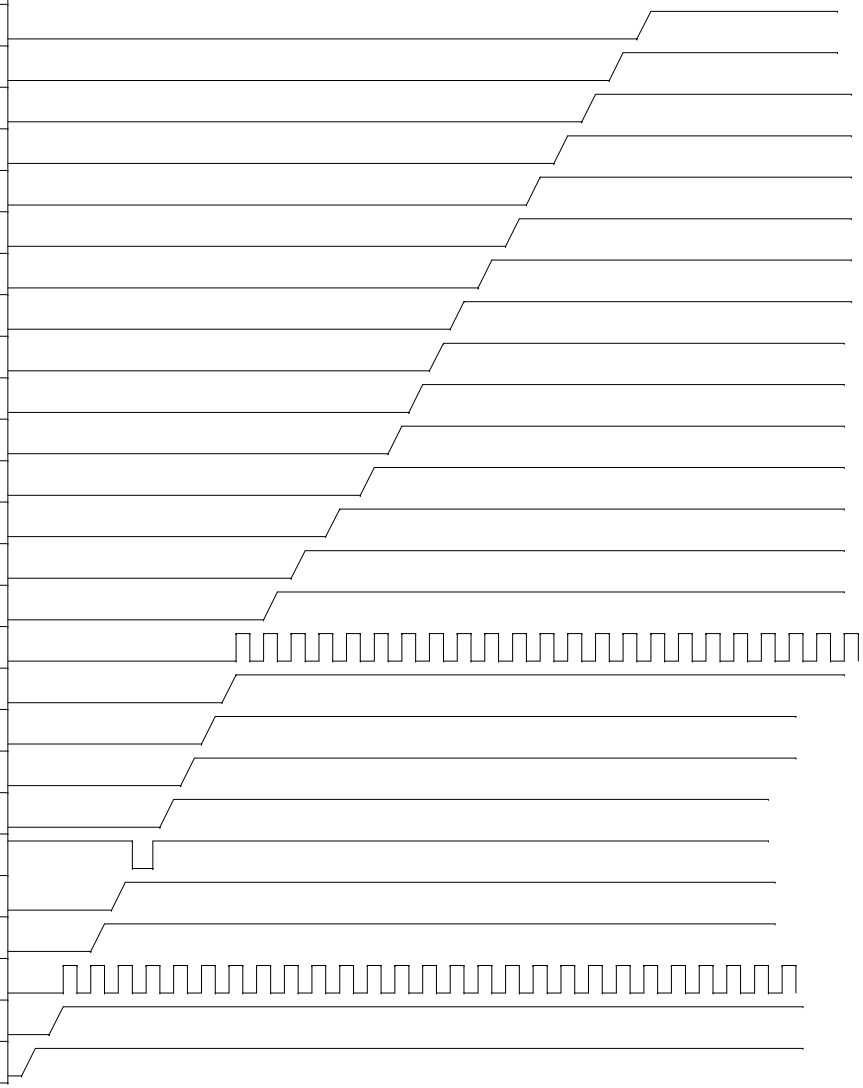
# POWER ON SEQUENCE

| Source | Destination | Signal Name |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |
| PCH | CPU | DMI Message |
| PCH | CPU/Board | PLTRST |
| CPU VRM | PCH | PCH_SYSPWROK |
| CPU VRM | CPU | V_CPU_CORE |
| CPU | CPU VRM | CPU SVID |
| PCH | CPU | H_DRAMPWRGD |
| Board | PCH | PWROK3 |
| Board | CPU VRM | PCH_1D05V_PG |
| Board | PCH | V_1P05_PCH/<br>V_1P5_PCH |
| Board | Board | +12V |
| Board | Board | VCC/VCC3 |
| Board | Board | V_SM |
| SIO | Board | SIO_PSON_N |
| PCH | Board | SLP_S3# |
| PCH | Board | SLP_S4# |
| PCH | Board | SUSCLK |
| Board | PCH | RSMRST# |
| Board | PCH | SB5V/SB3V |
| SIO | Board | SUS3V_ON#/<br>SUS5V_ON# |
| PCH | Board | SLP_SUS# |
| Board | PCH | PWR button |
| Board | PCH | DPWROK |
| Board | PCH | 5VA/3VA |
| Board | PCH | RTCCLK |
| Board | PCH | RTCRST# |
| Board | PCH | VccRTC |



<Variant Name>

| | | |
|---|---|---|
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| Title | TBD | |
| Size<br>B | Document Number<br>Rosa_Tigris AIO | Rev<br>1 |
| Date: Monday, January 06, 2014 | Sheet 7 of 58 | |

## Intel B75 GPIO

| GPIO | IC Pin Name | Power Well | Default | Signal Name | Usage | BIOS Programming S0 | S1 | S3 | S4 | S5 | Comment | Check | Signal Check? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GPIO[0] | SMBUSY# | Core | GPI | PECI_REQ_N | GPI (S_PECI_REQ#) | H | H | L | L | L | | | |
| GPIO[1] | - | Core | GPI | OSD_MENU | GPI (OSD_MENU Buttom) | active | H | L | L | L | L=press button<br>H=not press | | |
| GPIO[2] | PIRQE# | Core | GPI | W1_DETECT_USB | GPI (PCIE_MINI_CPUSB_DETECT#) | active | active | L | L | L | L=Detect<br>H=not Detect | | |
| GPIO[3] | PIRQF# | Core | GPI | OSD_UP | GPI (OSD_up and Enable BIST button) | active | H | L | L | L | L=Enable BIST fuction and press button | | |
| GPIO[4] | PIRQG# | Core | GPI | OSD_DN | GPI (OSD_down button) | active | H | L | L | L | L=press button<br>H=not press | | |
| GPIO[5] | PIRQH# | Core | GPI | W1_DETECT_PE | GPI (PCIE_MINI_CPPE_DETECT#) | active | active | L | L | L | L=Detect<br>H=not Detect | | |
| GPIO[6] | - | Core | GPI | PANEL_SEL2_CABLE_PCH | GPI (PANEL_SEL2_CABLE) | active | active | L | L | L | [PANEL_SEL1,PANEL_SEL2,PANEL_SEL3]<br>[1,1,1]=Samsung<br>[1,1,0]=Chimei<br>[1,0,1]=LG | | |
| GPIO[7] | - | Core | GPI | MB_SKU_ID2 | GPI (MB_SKU_ID2) | active | active | L | L | L | [MB_SKU_ID0,MB_SKU_ID1,MB_SKU_ID2]<br>[0,0,0]=UMA w/ Touch<br>[0,0,1]=UMA w/o Touch<br>[0,1,0]=GPU w/ Touch | | |
| GPIO[8] | - | Suspend | GPO | IGC_EN_N | GPI (IGC_EN_N and strap) | active | active | active | active | active | L=Enable<br>H=Disable | | |
| GPIO[9] | OC5# | Suspend | Native | USBOC1011* | Native (USB OC pin for REAR USB5,6) | default | default | default | default | default | | | |
| GPIO[10] | OC6# | Suspend | Native | USB_OC6_R_N | GPI (No used) | H | H | H | H | H | | | |
| GPIO[11] | SMBALERT# | Suspend | Native | LPC_PME_N | GPI(LPC_PME_N) | active | active | active | active | active | L=PME event occurs<br>H=No PME event | | |
| GPIO[12] | LAN_PHY_PWR_CTRL | Deep Sleep | Native | LAN_DISABLE_N | GPO (L_LAN_DISABLE#) | H | H | H | L | L | L=Disable<br>H=Enable<br>Depends on whether WOL is required | | |
| GPIO[13] | - | Suspend | GPI | Mini_Power_CTRL | GPO (CONTROL minicard power) | H | H | H | L | L | L=Disable<br>H=Enable<br>Depends on whether iSCT is required | | |
| GPIO[14] | OC7# | Suspend | Native | USB_OC7_R_N | GPI (No used) | H | H | H | H | H | L=interrupt<br>H=normal | | |
| GPIO[15] | - | Suspend | GPO | PCH_AUD_RST_N | GPO(PCH_AUD_LINK_RST_N) | H(condition) | H(condition) | L | L | L | L=mute<br>H=After finish the Audio verb post then driving H, and need to match vendor request sequence | | |
| GPIO[16] | SATA4GP | Core | GPI | SATA4GP | GPI (No used) | H | H | L | L | L | | | |
| GPIO[17] | - | Core | GPI | PANEL_SEL3_CABLE_PCH | GPI (PANEL_SEL3_CABLE) | active | active | L | L | L | [PANEL_SEL1,PANEL_SEL2,PANEL_SEL3]<br>[1,1,1]=Samsung<br>[1,1,0]=Chimei<br>[1,0,1]=LG | | |
| GPIO[18] | PCIECLKRQ1# | Core | Native | PCH_XDP_GP18 | GPI (No used) | L | L | L | L | L | | | |
| GPIO[19] | SATA1GP | Core | GPI | SATA1GP | GPI(strap) | H | H | L | L | L | | | |
| GPIO[20] | PCIECLKRQ2# | Core | Native | IO_SMI_N | GPI (SMI#) | active | active | active | L | L | L=interrupt<br>H=normal | | |
| GPIO[21] | SATA0GP | Core | GPI | BOARD_A | GPI (BOARD ID A) | active | active | L | L | L | [BOARD A,BOARD B,BOARD C]<br>[0,0,0]=PRE-SSI<br>[0,0,1]=SSI<br>[0,1,0]=PT<br>[0,1,1]=ST<br>[1,0,0]=A00<br>[1,0,1]=A01<br>[1,1,0]=A02<br>[1,1,1]=A03 | | |
| GPIO[22] | SCLOCK | Core | GPI | SMBUS_ISP | GPO (SMBUS control) | L | L | L | L | L | H=Simultaneous Mode<br>L=Isolate Mode<br>H to update DP translator firmware | | |
| GPIO[23] | LDRQ1# | Core | Native | TP_LPC_DRQ1_N | Native (L_DRQ1#) | default | default | default | default | default | | | |
| GPIO[24] | - | Suspend | GPO | H_SKTOCC_R_N | Native (H_SKTOCC#) | default | default | default | default | default | | | |
| GPIO[25] | PCIECLKRQ3# | Suspend | Native | LANCLK_REQ_N | Native (LANCLK_REQ) | default | default | default | default | default | | | |
| GPIO[26] | PCIECLKRQ4# | Suspend | Native | ME_CNTL | GPO (ME control) | H | H | H | H | H | use as ME control<br>H=Enable<br>L=Disable<br>ME_CNTL | | |
| GPIO[27] | - | Deep Sleep | GPI | PCH_GP27_PU | GPI (No used) | H | H | H | H | H | | | |
| GPIO[28] | - | Suspend | GPO | PCH_GP28_PU | GPI (No used) | H | H | H | H | H | | | |
| GPIO[29] | SLP_LAN# | Deep Sleep | Native | SLP_WLAN_N | Native (SLP_LAN#) | default | default | default | default | default | | | |
| GPIO[30] | SUSPWRDNACK /SUSWARN# | Suspend | Native | SUS_WARNB | Native (SUSWARN#) | default | default | default | default | default | | | |
| GPIO[31] | - | Deep Sleep | GPI | PW_CLEAR | GPI (PSWD_CLR) | active | active | active | active | active | L =Normal<br>H =Clear password | | |
| GPIO[32] | - | Core | GPO | MB_SKU_ID0 | GPI (MB_SKU_ID0) | active | active | L | L | L | [MB_SKU_ID0,MB_SKU_ID1,MB_SKU_ID2]<br>[0,0,0]=UMA w/ Touch<br>[0,0,1]=UMA w/o Touch<br>[0,1,0]=GPU w/ Touch | | |
| GPIO[33] | - | Core | GPO | PWRCN_DET_N | GPI (PWRCN_DET) | active | active | L | L | L | L=Detect<br>H=not Detect | | |
| GPIO[34] | | Core | GPI | ADAPTOR_PSID | GPI (Adaptor ID recognize) | active | active | L | L | L | Though GPIO to read adaptor ID | | |
| GPIO[35] | | Core | GPO | MB_SKU_ID1 | GPI (S_GPI_SKU1) | active | active | L | L | L | [MB_SKU_ID0,MB_SKU_ID1,MB_SKU_ID2]<br>[0,0,0]=UMA w/ Touch<br>[0,0,1]=UMA w/o Touch<br>[0,1,0]=GPU w/ Touch | | |
| GPIO[36] | SATA2GP | Core | GPI | SATA2GP | Native (strap pin) | default | default | default | default | default | | | |
| GPIO[37] | SATA3GP | Core | GPI | SATA3GP | Native (strap pin) | default | default | default | default | default | | | |
| GPIO[38] | SLOAD | Core | GPI | LVDS_DET_B* | GPI (LVDS Detect B) | active | active | L | L | L | L=Detect<br>H=not Detect<br>Note:Only if both GPIO 38 and 48 are low, LVDS is detected | | |
| GPIO[39] | SDATAOUT0 | Core | GPI | INV_DET* | GPI (Inverter Detect) | active | active | L | L | L | L=Detect<br>H=not Detect | | |
| GPIO[40] | OC1# | Suspend | Native | USB_OC1_R_N | GPI (No used) | H | H | H | H | H | | | |
| GPIO[41] | OC2# | Suspend | Native | USB_OC2_R_N | GPI (No used) | H | H | H | H | H | | | |
| GPIO[42] | OC3# | Suspend | Native | USB_OC3_R_N | GPI (No used) | H | H | H | H | H | | | |
| GPIO[43] | OC4# | Suspend | Native | USBOC89* | Native (USB OC pin for REAR USB3,4) | default | default | default | default | default | | | |
| GPIO[44] | PCIECLKRQ5# | Suspend | Native | INTRUDER_DET | GPI (INTRUDER CABLE Detect) | active | active | active | active | active | L=Detect<br>H=not Detect | | |
| GPIO[45] | PCIECLKRQ6# | Suspend | Native | COM_DET | GPI (COM Port detect) | active | active | active | active | active | L=Detect<br>H=not Detect | | |
| GPIO[46] | PCIECLKRQ7# | Suspend | Native | BOARD_B | GPI (BOARD ID B) | active | active | active | L | L | [BOARD A,BOARD B,BOARD C]<br>[0,0,0]=PRE-SSI<br>[0,0,1]=SSI<br>[0,1,0]=PT<br>[0,1,1]=ST<br>[1,0,0]=A00<br>[1,0,1]=A01<br>[1,1,0]=A02<br>[1,1,1]=A03 | | |
| GPIO[48] | SDATAOUT1 | Core | GPI | LVDS_DET_A* | GPI (LVDS Detect A) | active | active | L | L | L | L=Detect<br>H=not Detect<br>Note:Only if both GPIO 38 and 48 are low, LVDS is detected | | |
| GPIO[49] | SATA5GP | Core | GPI | SATA5GP | Native (SATA5GP) | default | default | default | default | default | | | |
| GPIO[50] | - | Core | GPI | BIST_DISABLE | GPO (BIST_DISABLE) | L | L | L | L | L | L=Default<br>H=Disable BIST | | |
| GPIO[51] | - | Core | GPO | P_GNT_N1 | GPI (strap pin) | H | H | L | L | L | | | |
| GPIO[52] | - | Core | GPI | TP_GPIO52 | GPO (No used) | L | L | L | L | L | | | |
| GPIO[53] | - | Core | GPO | P_GNT_N2 | GPI (strap pin) | H | H | L | L | L | | | |
| GPIO[54] | - | Core | GPI | TP_GPIO54 | GPO (No used) | L | L | L | L | L | | | |
| GPIO[55] | - | Core | GPO | P_GNT_N3 | GPI (strap pin) | H | H | L | L | L | | | |
| GPIO[57] | - | Suspend | GPI | BIST_ENABLE | GPO (BIST Enable) | active | active | active | L | L | H=Enable BIST<br>L=Default | | |
| GPIO[58] | SML1CLK# | Suspend | Native | SMLICLK_PCH | Native (SMLINK1_CLK) | default | default | default | default | default | | | |
| GPIO[59] | OC0# | Suspend | Native | USBOC01* | Native (USB OC pin for SIDE USB3.0) | default | default | default | default | default | | | |
| GPIO[60] | SML0ALERT# | Suspend | Native | MPCIE_DISABLE_N | GPO (WIRELESS_DISABLE#) | H | H | H | L | L | L=Disable<br>H=Enable | | |
| GPIO[61] | SUS_STAT# | Suspend | Native | SUS_STAT_N | Native(SUS_STAT#) | default | default | default | default | default | | | |
| GPIO[62] | SUSCLK | Suspend | Native | SUSCLK | Native (SUSCLK) | default | default | default | default | default | | | |
| GPIO[63] | SLP_S5# | Suspend | Native | SLP_S5_N | Native (Sleep S5) | default | default | default | default | default | | | |
| GPIO[64] | CLKOUTFLEX0 | Core | Native | CLKOUTFLEX0 | GPO (No used) | L | L | L | L | L | | | |
| GPIO[65] | CLKOUTFLEX1 | Core | Native | CLKOUTFLEX1 | Native (CLKOUTFLEX1) | default | default | default | default | default | Please configure to 48MHz clock | | |
| GPIO[66] | CLKOUTFLEX2 | Core | Native | CLKOUTFLEX2 | GPO (No used) | L | L | L | L | L | | | |
| GPIO[67] | CLKOUTFLEX3 | Core | Native | CK_14M_FLEX | Native (CK_14M_SIO) | default | default | default | default | default | Please configure to 14.318MHz clock | | |
| GPIO[68] | - | Core | GPI | BOARD_C | GPI (BOARD ID C) | active | active | L | L | L | [BOARD A,BOARD B,BOARD C]<br>[0,0,0]=PRE-SSI<br>[0,0,1]=SSI<br>[0,1,0]=PT<br>[0,1,1]=ST<br>[1,0,0]=A00<br>[1,0,1]=A01<br>[1,1,0]=A02<br>[1,1,1]=A03 | | |
| GPIO[69] | - | Core | GPI | WEBCAM_DET | GPI (WEBCAM DET) | active | active | L | L | L | L=Detect<br>H=not Detect | | |
| GPIO[70] | - | Core | Native | PANEL_SEL1_CABLE_PCH | GPI (PANEL_SEL1_CABLE) | active | active | L | L | L | [PANEL_SEL1,PANEL_SEL2,PANEL_SEL3]<br>[1,1,1]=Samsung<br>[1,1,0]=Chimei<br>[1,0,1]=LG | | |
| GPIO[71] | - | Core | Native | TP_DET | GPI (TOUCH_PANEL_DET) | active | active | L | L | L | L=Detect<br>H=not Detect | | |
| GPIO[72] | - | Deep Sleep | Native | PCH_AUD_MUTE | GPO (No used) | H | H | H | L | L | | | |
| GPIO[73] | PCIECLKRQ0# | Suspend | Native | PCH_GP73_PD | GPI (No used) | L | L | L | L | L | | | |
| GPIO[74] | SML1ALERT#/PCHHOT# | Suspend | Native | TMIN_SHIFT_P | Native (TMIN_SHIFT) | active | active | L | L | L | Used as Temp_Alert# to indicate SIO that temp is out of range | | |
| GPIO[75] | SML1DATA | Suspend | Native | SMLIDATA_PCH | Native (S_SMLINK1_DATA) | default | default | default | default | default | | | |

## SIO SMSC5555

| GPIO | PIN NAME | PIN OUT | Power well | Bufffer Type | Current Usage | Signal Name | EX-PU/PD |
|---|---|---|---|---|---|---|---|
| GP000 | GP000 | 4 | V3_S5 | IO4 | NC | NC | NA |
| GP001 | GP001 | 5 | V3_S5 | IO4 | NC | NC | NA |
| GP002 | GP002 | 7 | V3_S5 | IO4 | NC | NC | NA |
| GP003 | GP003 | 8 | V3_S5 | IO4 | NC | NC | NA |
| GP004 | SUSWARN# / GP004 | 70 | V3_S5 | IO4 | SUS_WARNB_R | S_SUSWARN# | NA |
| GP005 | (H_CPURST#) GP005 / PECI_REQUEST# | 22 | V3_S5 | IO4 | SIO_PECI_REQ_N | O_PECI_REQ# | 10k pull-up to +3V |
| GP006 | YELLOW# / GP006 | 25 | V3_S5 | IO8 | SIO_YELLOW | O_YELLOW# | 499 pull-up to +5V_S5 |
| GP007 | GREEN# / GP007 | 26 | V3_S5 | IO8 | SIO_GREEN | O_GREEN# | 499 pull-up to +5V_S5 |
| GP010 | SMBDAT2 / GP010 | 27 | V3_S5 | IO8 | SIO_SMBDAT2 | S_SML1DATA | 2.2k pull-up to +3V_S5 |
| GP011 | SMBCLK2 / GP011 | 28 | V3_S5 | IO8 | SIO_SMBCLK2 | S_SML1CLK | 2.2k pull-up to +3V_S5 |
| GP013 | DPWROK / GP013 | 30 | V3_S5 | IO4 | PCH_DPWROK | O_DPWROK | 10k pull-down to GND |
| GP014 | (TMIN_SHIFT) GP014 | 35 | V3_S5 | IO4 | TMIN_SHIFT | TMIN_SHIFT | 8.2k pull-up to +3V_S5<br>330k pull-down to GND (Dummy) |
| GP015 | PWRBTN# / GP015 | 36 | V3_S5 | IO4 | PWRBTN_N | O_PWRBTN#IN | 1k pull-up to +3V_DUAL (Dummy) |
| GP016 | PROCHOT_IN#/PROCHOT_OUT#/GP016 | 38 | V3_S5 | LVIOD24 | SIO_PROCHOT_R_N | H_PROCHOT# | 51ohm pull-up to H_CPU_VCCIO_RIG |
| GP017 | TACH1 / GP017 | 39 | V3_S5 | IO4 | CPU_FAN_TACH_SIO | O_SEN_CPUFAN | 1k pull-up to +3V |
| GP020 | TACH2 / GP020 | 40 | V3_S5 | IO4 | SYS_FAN_TACH_SIO | O_SEN_CHAFAN | 1k pull-up to +3V |
| GP021 | TACH3 / GP021 | 41 | V3_S5 | IO4 | NC | NC | NA |
| GP022 | PWM1 / GP022 | 49 | V3_S5 | IO4 | CPU_FAN_CTRL_SIO | O_CPUFAN_PWM | 4.7k pull-up to +3V |
| GP023 | PWM2 / GP023 | 50 | V3_S5 | IO4 | SYS_FAN_CTRL_SIO | O_CHAFAN_PWM | 4.7k pull-up to +3V |
| GP024 | PWM3 / GP024 | 51 | V3_S5 | IO4 | SIO_LVDS_BL_ADJ | NC | NA |
| GP025 | (FP_CBL_DET#) GP025 | 52 | V3_S5 | IO4 | FP_CBL_DET | O_FP_CBL_DET# | 8.2k pull-up to +3V_S5 |
| GP026 | PCI_RST_SYS# / GP026 | 53 | V3_S5 | IO4 | PCIRST1# | X_PLTRST_PCIE_SLOT# | NA |
| GP027 | PCI_RST_SLOTS# / GP027 | 54 | V3_S5 | IO4 | PCIRST2# | NC | NA |
| GP030 | PS_ON# / GP030 | 55 | V3_S5 | OD4 | SIO_PSON_N | O_PSON# | 4.7k pull-up to +5VSB |
| GP031 | (PC_SPKR_DET) GP031 | 56 | V3_S5 | IO4 | PC_SPKR_DET | O_AUD_PCSPKR_DET# | 8.2k pull-up to +3V_S5 |
| GP032 | SUS3V_FON# / GP032 | 58 | V3_S5 | IO4 | SUS3V_FON_N | O_SUS_3V_F_ON | NA |
| GP033 | PWR_GOOD_3V / GP033 | 59 | V3_S5 | IO4 | PWROK3_1 | PWRGD_3V | NA |
| GP034 | RSMRST#/ GP034 | 60 | V3_S5 | O4 | RSMRST_N | O_RSMRST# | NA |
| GP035 | LATCHED_BF_CUT / GP035 | 69 | V3_S5 | IO4 | NC | NC | NA |
| GP036 | GP036 / SMB_CLK1 | 72 | V3_S5 | IO8 | SMLICLK_PCH | NC | NA |
| GP040 | GP040 / SMB_DAT1 | 74 | V3_S5 | IO8 | SMLIDATA_PCH | NC | NA |
| GP041 | GP041 / IO_PME# | 77 | V3_S5 | IO4 | LPC_PME_N | O_PME# | 10k pull-up to +3V_S5 |
| GP042 | GP042 | 78 | V3_S5 | IO4 | NC | NC | NA |
| GP043 | DCD1# / GP043 | 98 | V3_S5 | IO4 | SP_DCD_N | O_DCD1#_R | NA |
| GP044 | DSR1# / GP044 | 99 | V3_S5 | IO4 | SP_DSR_N | O_DSR1#_R | NA |
| GP045 | RXD1 / GP045 | 100 | V3_S5 | IO4 | SP_RXD_N | O_RXD1_R | NA |
| GP046 | RTS1# / GP046 | 101 | V3_S5 | IO4 | SP_RTS_N | O_RTS1#_R | 10k pull-up to +3V |
| GP047 | (5V_PRSNT) GP047 / TXD1 | 102 | V3_S5 | IO8 | SP_TXD_SIO | O_TXD1_R_C | 10k pull-up to +3V |
| GP050 | CTS1# / GP050 | 103 | V3_S5 | IO4 | SP_CTS_N | O_CTS1#_R | NA |
| GP051 | DTR1# / GP051 | 104 | V3_S5 | IO4 | SP_DTR_N | O_DTR1#_R | NA |
| GP052 | RI1# / GP052 | 105 | V3_S5 | IO4 | SP_RI_N | O_RI1#_R | NA |
| GP053 | GP053 | 107 | V3_S5 | IO4 | OCP8 | NC | NA |
| GP054 | GP054 | 108 | V3_S5 | IO4 | NC | NC | NA |
| GP055 | GP055 | 109 | V3_S5 | IO4 | NC | NC | NA |
| GP056 | (PWR2_PRSNT) GP056 | 110 | V3_S5 | IO4 | PWR2_PRSNT | O_PWR2_PRSNT | 10k pull-up to +3V |
| GP057 | (MEM_REG_PG) GP057 | 111 | V3_S5 | IO8 | MB_REG_PG | O_MB_REG_PG | 10k pull-up to +3V |
| GP060 | GP060 | 112 | V3_S5 | IO4 | NC | NC | NA |
| GP061 | (MEM_REG_PG) GP061 | 113 | V3_S5 | IO4 | MEM_REG_PG | O_MEM_REG_PG | 10k pull-up to +3V |
| GP062 | GP062 | 114 | V3_S5 | IO4 | GPU_THREMAL_INT | NC | NA |
| GP063 | GP063 / KBDRST# | 120 | V3_S5 | IO4 | KBRST_N | O_KB_RST# | 10k pull-up to +3V |
| GP064 | GP064 / A20M | 121 | V3_S5 | IO4 | A20GATE | O_A20GATE | 10k pull-up to +3V |
| GP066 | SLP_S5# / GP066 | 124 | V3_S5 | IO4 | SLP_S4_SIO | S_SLP_S5# | NA |
| GP070 | SPEAKER [DIAG_EN#] / GP070 | 127 | V3_S5 | IO4 | SIO_SPKR | O_SPEAKER | 8.2k pull-up to +3V_S5(dummy)<br>8.2k pull-down to GND |
| GP071 | (SLP_M#) GP071 / IO_SMI# | 128 | V3_S5 | IO4 | IO_SMI_N | S_SLP_M# | NA |
| GP075 | SUS5V_ON# / GP075 | 75 | V3_S5 | IO4 | SUS5V_ON_N | O_SUS_5VON | 22k pull-up to +5VSB |
| GP076 | SUS3V_ON# / GP076 | 76 | V3_S5 | IO4 | SUS3V_ON_N | O_SUS_3V_ON | NA |
| GP100 | DDC_DAT_5V / GP100 | 84 | V3_S5 | IO12 | NC | NC | NA |
| GP101 | DDC_DAT_25V / GP101 | 85 | V3_S5 | IO12 | NC | NC | NA |
| GP102 | DDC_CLK_5V / GP102 | 86 | V3_S5 | IO12 | NC | NC | NA |
| GP103 | DDC_CLK_25V / GP103 | 87 | V3_S5 | IO12 | NC | NC | NA |
| GP104 | GP104 | 88 | V3_S5 | IO12 | NC | NC | NA |
| GP105 | GP105 | 89 | V3_S5 | IO12 | NC | NC | NA |
| GP106 | GP106 | 90 | V3_S5 | IO12 | NC | NC | NA |
| GP107 | GP107 | 91 | V3_S5 | IO12 | SIO_HDD_LED | NC | NA |
| GP111 | GP111 | 63 | V3_S5 | IO4 | NC | NC | NA |
| GP112 | GP112 | 64 | V3_S5 | IO4 | NC | NC | NA |
| GP113 | GP113 | 65 | V3_S5 | IO4 | NC | NC | NA |
| GP114 | GP114 | 66 | V3_S5 | IO4 | NC | NC | NA |
| GP116 | BACKFEED_CUT# / GP116 | 97 | V3_S5 | IO12 | NC | NC | NA |
| GP117 | GP117 | 15 | V3_S5 | IO4 | NC | NC | NA |
| GP120 | SDAT_1 / GP120 | 80 | V3_S5 | IO8 | SMB_DATA_RESUME | S_SMBDATA_RESUME | 2.2k pull-up to +3V_S5 |
| GP121 | SDAT / GP121 | 81 | V3_S5 | IO8 | SMB_DATA_MAIN | S_SMBDATA_MAIN | 2.7k pull-up to +3V |
| GP122 | SCLK_1 / GP122 | 82 | V3_S5 | IO8 | SMB_CLK_RESUME | S_SMBCLK_RESUME | 2.2k pull-up to +3V_S5 |
| GP123 | SCLK / GP123 | 83 | V3_S5 | IO8 | SMB_CLK_MAIN | S_SMBCLK_MAIN | 2.7k pull-up to +3V |
| GP124 | PCIAUX_CTRL# / GP124 | 93 | V3_S5 | IO8 | NC | O_PCIAUX_CTRL | NA |
| GP125 | PCIAUX_GATE / GP125 | 94 | V3_S5 | IO8 | NC | O_PCIAUX_GATE | NA |
| GP126 | GP126 | 95 | V3_S5 | IO4 | NC | NC | NA |
| GP127 | SUS_ACK_EN# / GP127 | 96 | V3_S5 | IO12 | SUS_ACK_EN_N | O_SUS_ACK_EN# | NA |

*Current Usage definition:
I: used as GPI
O: used as GPO
NU: not used
Native: used as native function
Strapping: used as strapping function

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPIO TABLE

| Size | Document Number | Rev |
|---|---|---|
| D | Rosa_Tigris AIO | 1 |

Date: Monday, January 06, 2014

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title TBD

| Size | Document Number | Rev |
|---|---|---|
| C | Rosa_Tigris AIO | 1 |

Date: Monday, January 06, 2014 Sheet 9 of 58

## CLOCK

19 CK_PE_100M_MCP_DP
19 CK_PE_100M_MCP_DN

## CPU_VCORE

42 VCC_SENSE
42 VSS_SENSE
42 H_VIDSCK_VR
42 H_VIDSOUT_VR
42 H_VIDALERT_N_VR

## XDP

14 H_TDO
14 H_TDI
14 H_TCK
14 H_TMS
14 H_TRST_N
14 H_PRDY_N
14 H_PREQ_N
14 XDP_DBRESET_N
14 HSW_XDP_MBP_0
14 HSW_XDP_MBP_1
14 HSW_PCUDEBUG_0
14 HSW_PCUDEBUG_1
14 HSW_PCUDEBUG_2
14 HSW_PCUDEBUG_3
14 HSW_PCUDEBUG_4
14 HSW_PCUDEBUG_5
14 HSW_PCUDEBUG_6
14 HSW_PCUDEBUG_7
14 HSW_PCUDEBUG_8
14 HSW_PCUDEBUG_9
14 HSW_PCUDEBUG_10
14 HSW_PCUDEBUG_11
14 HSW_PCUDEBUG_12
14 HSW_PCUDEBUG_13
14 HSW_PCUDEBUG_14
14 HSW_PCUDEBUG_15
14 HSW_PCUSTB_0_DP
14 HSW_PCUSTB_0_DN
14 HSW_PCUSTB_1_DP
14 HSW_PCUSTB_1_DN
10 H_CPURST_N
14 XDP_PWR_DEBUG

## OTHER

10 H_CPURST_N
13 VCCST
14,18 H_PWRGD
21,37 PLTRST_N
18 H_SKTOCC_N
18 FP_RST_PCH_N
18 H_DRAMPWRGD
19 CK_DPNS_R_DN
19 CK_DPNS_R_DP
14,18,37,42 VR_READY
20 H_PM_SYNC_0
20 CPU_THERMTRIP_N
20,37 H_PECI
14,20 PLTRST_CPU_N
37,42 H_PROCHOT_N
37,42 H_PROCHOT_R_N

MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SIGNAL PAGE
PLACE IN CRB AREA

H_VIDSCK_VR — R745 1 0R0402-PAD-2-GP — H_VIDSCK
H_VIDSOUT_VR — R770 1 0R0402-PAD-2-GP — H_VIDSOUT
H_VIDALERT_N_VR — R742 1 0R0402-PAD-2-GP — H_VIDALERT_N

V_CPU_VCCIO_RIGHT
R749 1 75R2F-2-GP
R769 1 110R2F-GP
R767 1 (R) 90D9R2F-1-GP

H_VIDSCK
H_VIDSOUT
H_VIDALERT_N — R746 1 44D2R2F-GP
R768 2 100R2F-L1-GP-U
H_DRAMPWRGD — R764 1 0R0402-PAD-2-GP

PLTRST_CPU_N — 1 R72 2 0R0402-PAD-2-GP
(R) R63 665R2F-2-GP
(R) R61 43R2J-GP
Joey_SC_0916
C38 SCD1U16V2KX-3GP
TPAD28 TP60
2010/12/20 SB Add EMI Cap
03/21:follow CRB1.0 rout the CFG[0] to XDP !

## Defensive Design

V_CPU_VCCIO_RIGHT
R62 75R2F-2-GP (R)
PLTRST_CPU_N2
VR_READY — R55 1 (R) 2 150KR2J-GP
PLTRST_N — R59 1 (R) 2 1K3R2F-1-GP
(R) C25 SC100P50V2JN-3GP
PLTRST_N_R — 2 Q11A MMBT3904DW-1-GP (R75.03904.07C)
Q11B MMBT3904DW-1-GP (R75.03904.07C) 5 — PLTRST_CPU_N1 — R57 2 (R) 1 100KR2J-1-GP — SB3V

Joey_SA_0417
FP_RST_PCH_N — R744 1 0R0402-PAD-2-GP
XDP_DBRESET_N
R828 1 49D9R2F-GP
TPAD28 TP99
TPAD28 TP94

CPU1E — HASWELL — HASWEINFU — 5 OF 10

| CPU1E | | | |
|---|---|---|---|
| CK_PE_100M_MCP_DN | V4 | BCLK# | |
| CK_PE_100M_MCP_DP | V5 | BCLK | |
| H_VIDSCK | C38 | VIDSCLK | |
| H_VIDSOUT | C37 | VIDSOUT | |
| H_VIDALERT_N | B37 | VIDALERT# | |
| H_DRAMPWRGD_CPU | AK21 | SM_DRAMPWROK | |
| H_PWRGD | AB35 | PWRGOOD | |
| H_CPURST_N | M39 | RESET# | |
| H_PM_SYNC_0 | P36 | PM_SYNC | |
| H_PECI | N37 | PECI | |
| TP_H_CATERR_N | M36 | CATERR# | |
| H_PROCHOT_R_N | K38 | PROCHOT# | |
| CPU_THERMTRIP_N | F37 | THERMTRIP# | |
| H_SKTOCC_N | D38 | SKTOCC# | |
| DIMM_CA_CPU_VREF_A | AB38 | SM_VREF | |
| HSW_PCUDEBUG_0 | AA37 | CFG0 | |
| HSW_PCUDEBUG_1 | Y38 | CFG1 | |
| HSW_PCUDEBUG_2 | AA36 | CFG2 | |
| HSW_PCUDEBUG_3 | W38 | CFG3 | |
| HSW_PCUDEBUG_4 | V39 | CFG4 | |
| HSW_PCUDEBUG_5 | U39 | CFG5 | |
| HSW_PCUDEBUG_6 | U40 | CFG6 | |
| HSW_PCUDEBUG_7 | V38 | CFG7 | |
| HSW_PCUDEBUG_8 | T40 | CFG8 | |
| HSW_PCUDEBUG_9 | Y35 | CFG9 | |
| HSW_PCUDEBUG_10 | AA34 | CFG10 | |
| HSW_PCUDEBUG_11 | V37 | CFG11 | |
| HSW_PCUDEBUG_12 | Y34 | CFG12 | |
| HSW_PCUDEBUG_13 | U38 | CFG13 | |
| HSW_PCUDEBUG_14 | W34 | CFG14 | |
| HSW_PCUDEBUG_15 | V35 | CFG15 | |
| HSW_PCUSTB_0_DP | Y36 | | |
| HSW_PCUSTB_0_DN | Y37 | CFG17 | |
| HSW_PCUSTB_1_DP | V36 | CFG16 | |
| HSW_PCUSTB_1_DN | W36 | CFG19 | |
| | | CFG18 | |
| H_TCK | D39 | TCK | |
| H_TDI | F38 | TDI | |
| H_TDO | F39 | TDO | |
| H_TMS | E39 | TMS | |
| H_TRST_N | E37 | TRST# | |
| H_PRDY_N | L39 | PRDY# | |
| H_PREQ_N | L37 | PREQ# | |
| XDP_DBRESET_N | G40 | DBR# | |
| TESTLOW_2 | N5 | TESTLO_N5 | |
| TP_RSVD_K8 | K8 | RSVD_TP_K8 | |
| TP_RSVD_J10 | J10 | RSVD_TP_J10 | |

| CPU1E | | | |
|---|---|---|---|
| BPM#0 | G39 | HSW_XDP_MBP_0 | |
| BPM#1 | J39 | HSW_XDP_MBP_1 | |
| BPM#2 | G38 | TP_CPU_G38 | TP59 TPAD28 |
| BPM#3 | H37 | TP_CPU_H37 | TP54 TPAD28 |
| BPM#4 | H38 | TP_CPU_H38 | TP46 TPAD28 |
| BPM#5 | J38 | TP_CPU_J38 | TP51 TPAD28 |
| BPM#6 | K39 | TP_CPU_K39 | TP57 TPAD28 |
| BPM#7 | K37 | TP_CPU_K37 | TP50 TPAD28 |
| RSVD_T35 | T35 | TP_CPU_T35 | TP44 TPAD28 |
| RSVD_M38 | M38 | TP_CPU_M38 | TP43 TPAD28 |
| TESTLO_P6 | P6 | TESTLOW_1 | R829 1 49D9R2F-GP |
| RSVD_K9 | K9 | VCCST | |
| RSVD_H15 | H15 | TP_RSVD_H15 | TP76 TPAD28 |
| RSVD_J9 | J9 | TP_RSVD_J9 | TP98 TPAD28 |
| RSVD_H14 | H14 | TP_RSVD_H14 | TP77 TPAD28 |
| VCC_M8 | M8 | | V_CPU_CORE |
| RSVD_AV2 | AV2 | TP_RSVD_AV2 | TP107 TPAD28 |
| RSVD_TP_J16 | J16 | TP_RSVD_J16 | TP74 TPAD28 |
| RSVD_TP_H16 | H16 | TP_RSVD_H16 | TP75 TPAD28 |
| PWR_DEBUG | N40 | PWR_DEBUG | |
| VSS | N39 | | |
| VSS | V7 | TP_RSVD_V7 | TP95 TPAD28 Joey_SA_0417 |
| VSS | AB6 | TP_RSVD_AB6 | TP101 TPAD28 |
| VSS | K13 | TP_RSVD_K13 | |
| RSVD_TP_K13 | J8 | TP_RSVD_J8 | TP100 TPAD28 |
| RSVD_TP_J8 | R1 | DDR_RCOMP_0 | R145 1 100R2F-L1-GP-U |
| SM_RCOMP0 | P1 | DDR_RCOMP_1 | R146 1 75R2F-2-GP |
| SM_RCOMP1 | R2 | DDR_RCOMP_2 | R147 1 100R2F-L1-GP-U |
| SM_RCOMP2 | AB36 | TP_RSVD_AB36 | TP40 TPAD28 |
| RSVD_AB36 | AW2 | TP_RSVD_AW2 | TP105 TPAD28 |
| RSVD_TP_AW2 | AV1 | TP_RSVD_AV1 | TP109 TPAD28 |
| RSVD_TP_AV1 | AC8 | TP_RSVD_AC8 | TP93 TPAD28 |
| RSVD_AC8 | P4 | | V_VCCIOA_LOAD |
| VCOMP_OUT | U8 | TP_RSVD_U8 | TP91 TPAD28 |
| RSVD_U8 | AB33 | TP_RSVD_AB33 | TP61 TPAD28 |
| RSVD_AB33 | T8 | CPU_VSS_T8 | TP97 TPAD28 Joey_SA_0418 |
| RSVD_T8 | Y8 | TP_RSVD_Y8 | TP96 TPAD28 |
| RSVD_Y8 | M10 | TP_RSVD_M10 | TP83 TPAD28 |
| RSVD_M10 | L10 | TP_RSVD_L10 | TP92 TPAD28 |
| RSVD_L10 | M11 | TP_RSVD_M11 | TP85 TPAD28 |
| RSVD_M11 | L12 | TP_RSVD_L12 | TP80 TPAD28 |
| RSVD_L12 | W8 | TP_RSVD_W8 | TP90 TPAD28 |
| RSVD_W8 | R33 | TP_RSVD_R33 | TP62 TPAD28 |
| RSVD_R33 | P33 | TP_RSVD_P33 | TP63 TPAD28 |
| RSVD_P33 | E40 | VCC_SENSE | |
| VCC_SENSE | | | (R) R71 49D9R2F-GP |
| VSS | N33 | | |
| VSS | J11 | | |
| VSS | M9 | | |
| VSS | J7 | | |
| VSS | F40 | VSS_SENSE | |
| VSS_SENSE | | | |
| RSVD_N35 | N35 | V_1P05_PECI_VCOM | TP41 TPAD28 |
| DPLL_REF_CLK# | W6 | CK_DPNS_R_DN | |
| DPLL_REF_CLK | W5 | CK_DPNS_R_DP | |
| CFG_RCOMP | H40 | TPEV_CFG_RCOMP | |

R728 49D9R2F-GP

V_SM — R757 1 1K8R2F-GP — H_DRAMPWRGD
R765 3K3R2J-3-GP

R58 1 10KR2J-3-GP — H_PWRGD
C26 2 1 SCD1U16V2KX-3GP
Joey_SC_0916

V_CPU_VCCIO_RIGHT
R774 51R2J-2-GP
H_PROCHOT_N — R743 1 0R0402-PAD-2-GP — H_PROCHOT_R_N

DIMM_CA_CPU_VREF_A — Joey_SA_0417 Remove 2.2ohm
R740 1 0R0402-PAD-2-GP — DIMM_CA_VREF_A — DIMM_CA_VREF_A 15
R741 1 0R0402-PAD-2-GP — DIMM_CA_VREF_B — DIMM_CA_VREF_B 16
C413 SCD022U16V2KX-3GP
DIMM_CA_CPU_VREF_RC
R758 24D9R2F-L-GP

## DEFENSIVE DESIGN PWR_DEBUG

R74 1 0R0402-PAD-2-GP

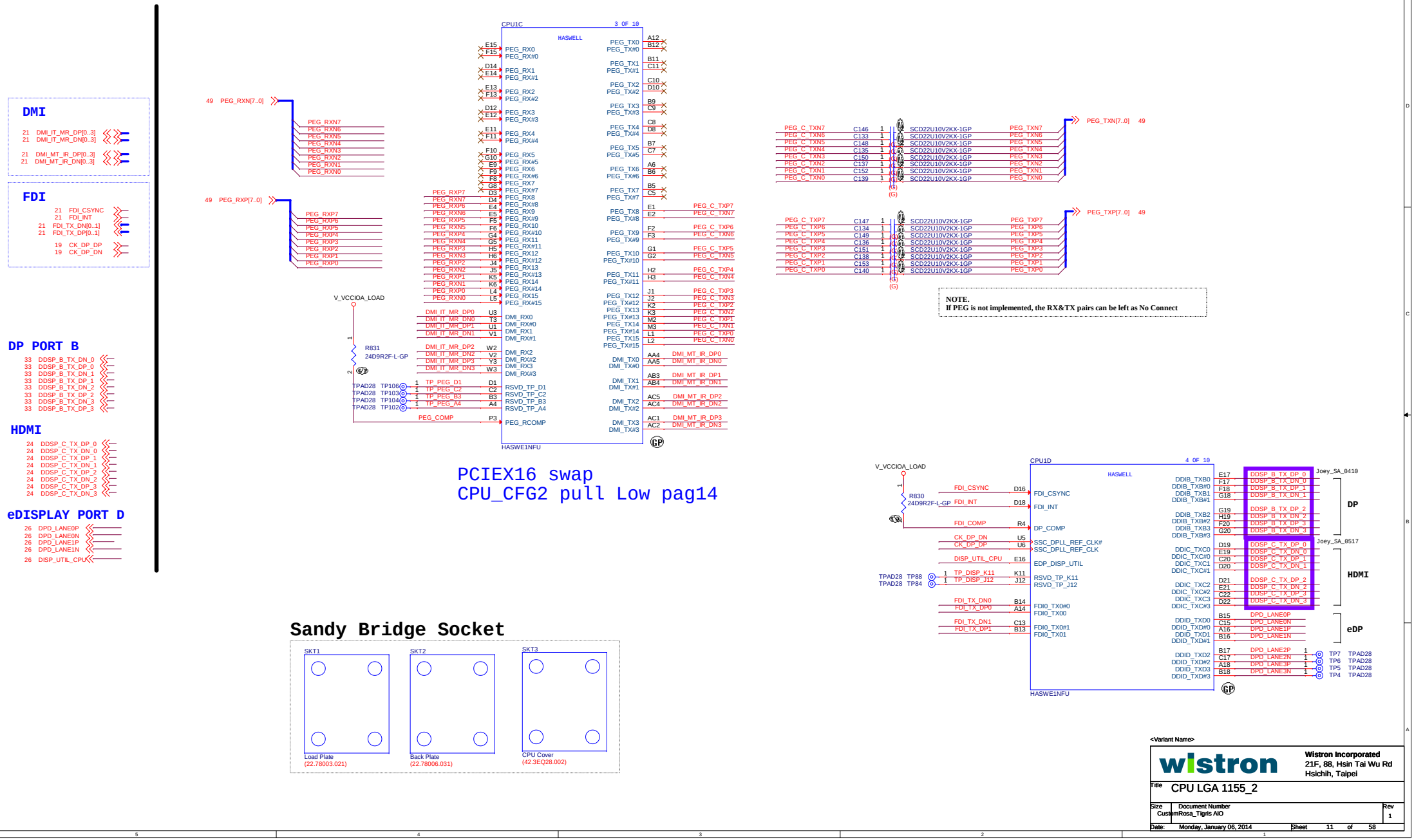
VCC3
R35 10KR2F-2-GP (R)
XDP_PWR_DEBUG — R38 1 (R) 2 10KR2F-2-GP
VR_READY — R42 1 (R) 2 10KR2F-2-GP
V_CPU_CORE — R47 1 (R) 2 10KR2F-2-GP

PWR_DEBUG_N
(R) R51 0R2J-2-GP
(R) C20 SCD1U16V2KX-3GP
MMBT3904DW-1-GP

VCC3
R37 10KR2F-2-GP (R)
PWR_DEBUG
(R75.03904.07C) Q9A
(R75.03904.07C) Q9B
PWR_DEBUG_1
MMBT3904DW-1-GP

V_1P05_PCH — R73 1 150R2F-1-GP — PWR_DEBUG
R64 2 (R) 1 10KR2J-3-GP

Joey_SA_0417 Remove FP_RST_DBR_N


DMI
21 DMI_IT_MR_DP[0..3]
21 DMI_IT_MR_DN[0..3]
21 DMI_MT_IR_DP[0..3]
21 DMI_MT_IR_DN[0..3]
FDI
21 FDI_CSYNC
21 FDI_INT
21 FDI_TX_DN[0..1]
21 FDI_TX_DP[0..1]
19 CK_DP_DP
19 CK_DP_DN
DP PORT B
33 DDSP_B_TX_DN_0
33 DDSP_B_TX_DP_0
33 DDSP_B_TX_DN_1
33 DDSP_B_TX_DP_1
33 DDSP_B_TX_DN_2
33 DDSP_B_TX_DP_2
33 DDSP_B_TX_DN_3
33 DDSP_B_TX_DP_3
HDMI
24 DDSP_C_TX_DP_0
24 DDSP_C_TX_DN_0
24 DDSP_C_TX_DP_1
24 DDSP_C_TX_DN_1
24 DDSP_C_TX_DP_2
24 DDSP_C_TX_DN_2
24 DDSP_C_TX_DP_3
24 DDSP_C_TX_DN_3
eDISPLAY PORT D
26 DPD_LANE0P
26 DPD_LANE0N
26 DPD_LANE1P
26 DPD_LANE1N
26 DISP_UTIL_CPU
CPU1C
3 OF 10
HASWELL
HASWE1NFU
49 PEG_RXN[7..0]
49 PEG_RXP[7..0]
V_VCCIOA_LOAD
R831
24D9R2F-L-GP
TPAD28 TP106
TPAD28 TP103
TPAD28 TP104
TPAD28 TP102
TP_PEG_D1
TP_PEG_C2
TP_PEG_B3
TP_PEG_A4
PEG_COMP
PEG_TXN[7..0] 49
PEG_TXP[7..0] 49
SCD22U10V2KX-1GP
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect
PCIEX16 swap
CPU_CFG2 pull Low pag14
V_VCCIOA_LOAD
R830
24D9R2F-L-GP
FDI_CSYNC
FDI_INT
FDI_COMP
CK_DP_DN
CK_DP_DP
DISP_UTIL_CPU
TPAD28 TP88
TPAD28 TP84
TP_DISP_K11
TP_DISP_J12
FDI_TX_DN0
FDI_TX_DP0
FDI_TX_DN1
FDI_TX_DP1
CPU1D
4 OF 10
HASWELL
HASWE1NFU
Joey_SA_0410
Joey_SA_0517
DP
HDMI
eDP
TP7 TPAD28
TP6 TPAD28
TP5 TPAD28
TP4 TPAD28
Sandy Bridge Socket
SKT1
SKT2
SKT3
Load Plate
(22.78003.021)
Back Plate
(22.78006.031)
CPU Cover
(42.3EQ28.002)
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CPU LGA 1155_2
Size
Custom
Document Number
Rosa_Tigris AIO
Rev
1
Date:
Monday, January 06, 2014
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of
58

## DDR DATA

15 M_DATA_A[0..63]
16 M_DATA_B[0..63]

15 M_DQS_A_DP[0..7]
15 M_DQS_A_DN[0..7]

16 M_DQS_B_DP[0..7]
16 M_DQS_B_DN[0..7]

## DDR CMD/ADD

15 M_MAA_A[0..15]
16 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

16 M_WE_B_N
16 M_CAS_B_N
16 M_RAS_B_N
16 M_SBS_B0
16 M_SBS_B1
16 M_SBS_B2

## DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1

15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

16 M_SCS_B_N0
16 M_SCS_B_N1

16 M_SCKE_B0
16 M_SCKE_B1

16 M_ODT_B0
16 M_ODT_B1

## DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

16 CK_M_DDR0_B_DP
16 CK_M_DDR0_B_DN
16 CK_M_DDR1_B_DP
16 CK_M_DDR1_B_DN

## DDR OTHERS

15,16 DDR3_DRAMRST_N

16 DIMM_DQ_CPU_VREF_B
15 DIMM_DQ_CPU_VREF_A

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU LGA 1155_3

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

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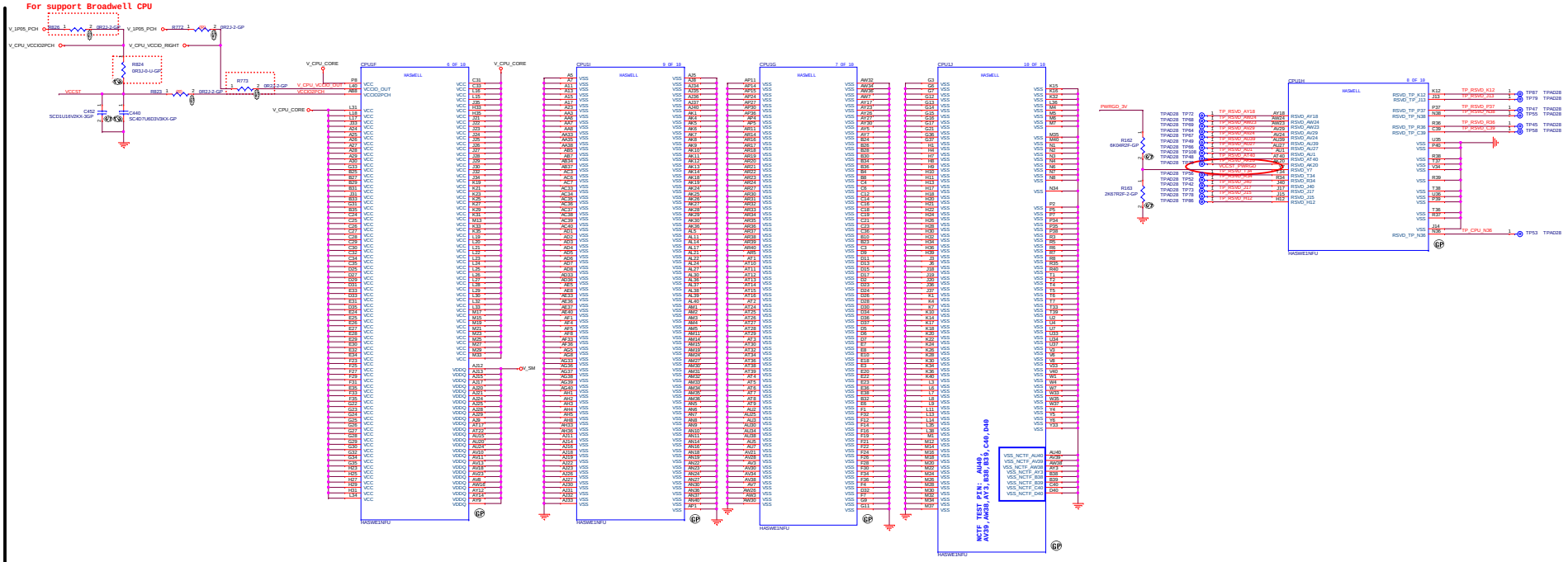


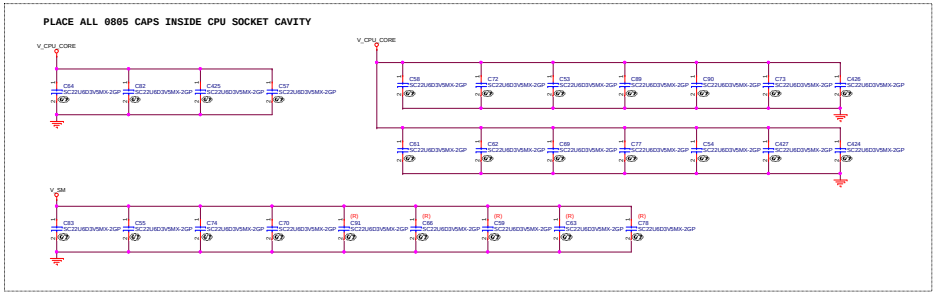


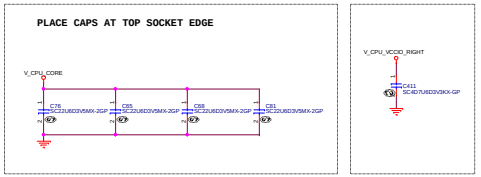


CPU Power Capacitor Quantity

| Net | CAP | AMOUNT |
|---|---|---|
| Vcore | 22uf 0805 | 22 |
| V_SM | 22uf 0805 | 4+5(R) |

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU LGA 1155_4

Size: Custom | Document Number: Rev: 1

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## XDP for CPU

10 H_TDO
10 H_TDI
10 H_TMS
10 H_TCK
10 H_TRST_N
10 H_PREQ_N
10 H_PRDY_N
10 XDP_DBRESET_N
10,18 H_PWRGD

10 HSW_PCUDEBUG_0
10 HSW_PCUDEBUG_1
10 HSW_PCUDEBUG_2
10 HSW_PCUDEBUG_3
10 HSW_PCUDEBUG_4
10 HSW_PCUDEBUG_5
10 HSW_PCUDEBUG_6
10 HSW_PCUDEBUG_7
10 HSW_PCUDEBUG_8
10 HSW_PCUDEBUG_9
10 HSW_PCUDEBUG_10
10 HSW_PCUDEBUG_11
10 HSW_PCUDEBUG_12
10 HSW_PCUDEBUG_13
10 HSW_PCUDEBUG_14
10 HSW_PCUDEBUG_15

10 HSW_XDP_MBP_0
10 HSW_XDP_MBP_1

10 HSW_PCUSTB_0_DP
10 HSW_PCUSTB_0_DN
10 HSW_PCUSTB_1_DP
10 HSW_PCUSTB_1_DN

10 XDP_PWR_DEBUG

15,16,26,37,50 SMB_DATA_MAIN
15,16,26,37,50 SMB_CLK_MAIN

22 HSW_STRAP_13

19 CK_100M_CPU_XDP_DN
19 CK_100M_CPU_XDP_DP

10,20 PLTRST_CPU_N

## APS CONNECTOR

18,37,39,42,45,47,48 SLP_S3_N
18,37,45,46 SLP_S4_N
18 PCH_SLP_M_N

## XDP for PCH

18,29 LANCLK_REQ_N
18 PCH_JTAG_RST_R
18 PCH_JTAG_TDO
18 PCH_JTAG_TDI
18 PCH_JTAG_TMS
18 PCH_JTAG_TCK

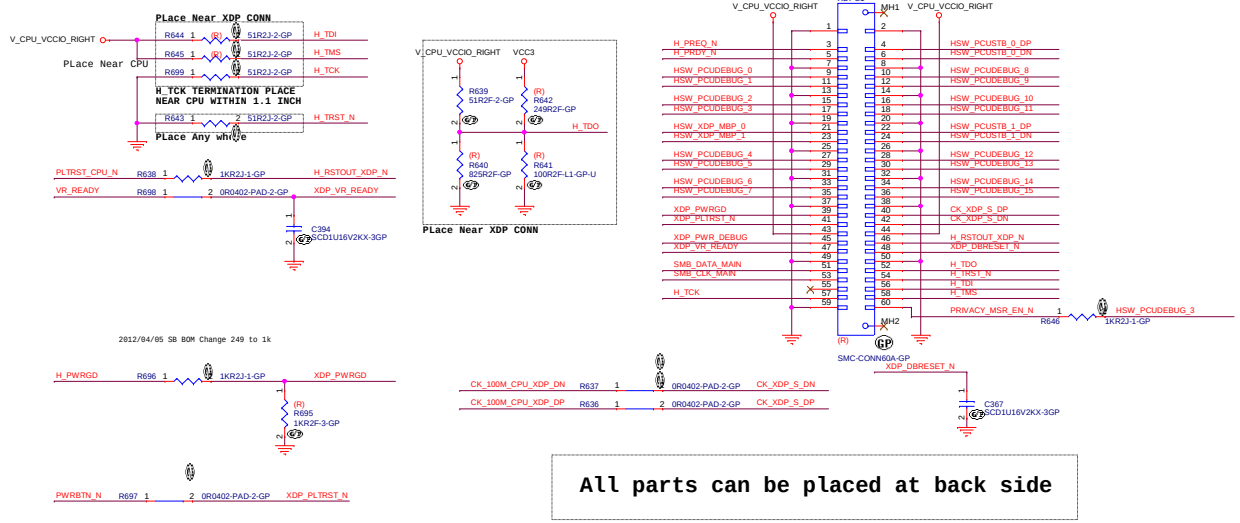
18,34,37 PWRBTN_N
18,22 IGC_EN_N

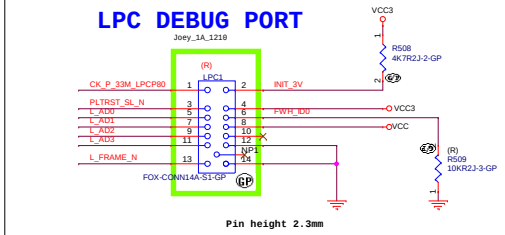
10,18,37,42 VR_READY

## LPC DEBUG PORT

18,36,37 L_AD0
18,36,37 L_AD1
18,36,37 L_AD2
18,36,37 L_AD3
18,36,37 L_FRAME_N
19 CK_P_33M_LPCP80

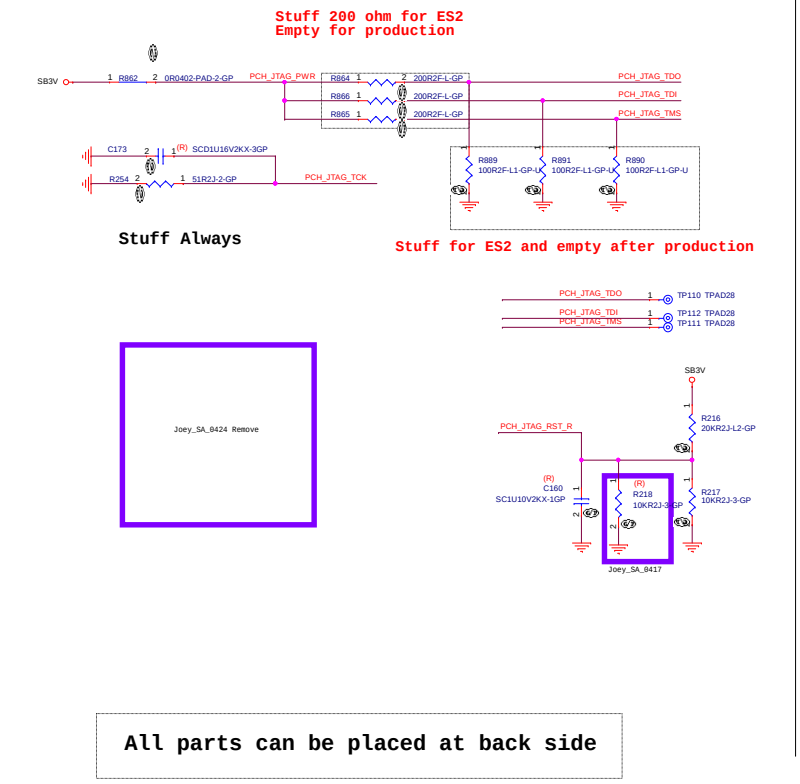
36,37,49,52 PLTRST_SL_N

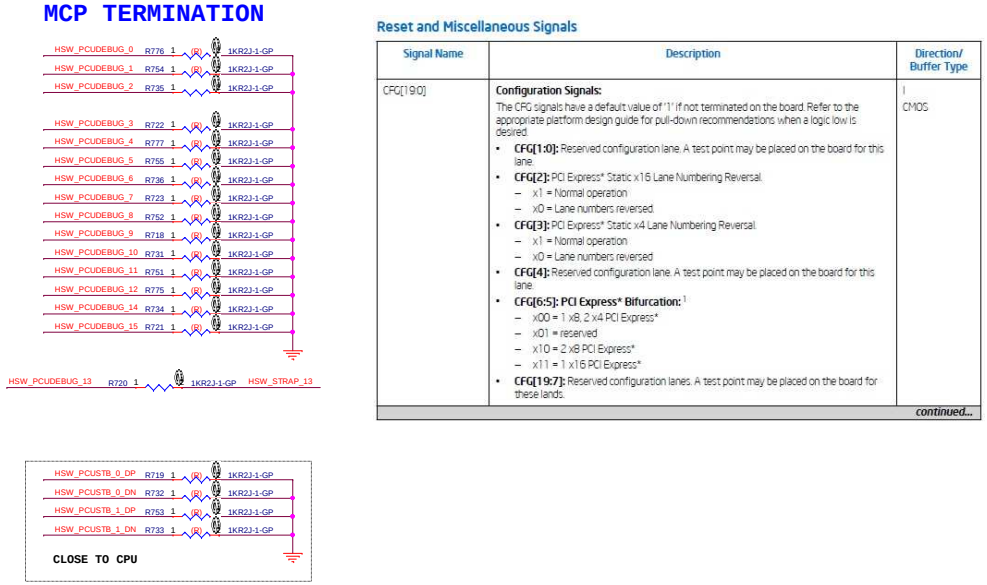



## APS CONNECTOR

PCH_SLP_M_N 1 TP117 TPAD28




### Reset and Miscellaneous Signals

| Signal Name | Description | Direction/ Buffer Type |
|---|---|---|
| CFG[19:0] | **Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.<br>• **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane.<br>• **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.<br>– x1 = Normal operation<br>– x0 = Lane numbers reversed.<br>• **CFG[3]:** PCI Express* Static x4 Lane Numbering Reversal.<br>– x1 = Normal operation<br>– x0 = Lane numbers reversed<br>• **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane.<br>• **CFG[6:5]: PCI Express* Bifurcation:** [1]<br>– x00 = 1 x8, 2 x4 PCI Express*<br>– x01 = reserved<br>– x10 = 2 x8 PCI Express*<br>– x11 = 1 x16 PCI Express*<br>• **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands. | I<br>CMOS |

*continued...*


<Variant Name>
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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: XDP/80 PORT HEADER
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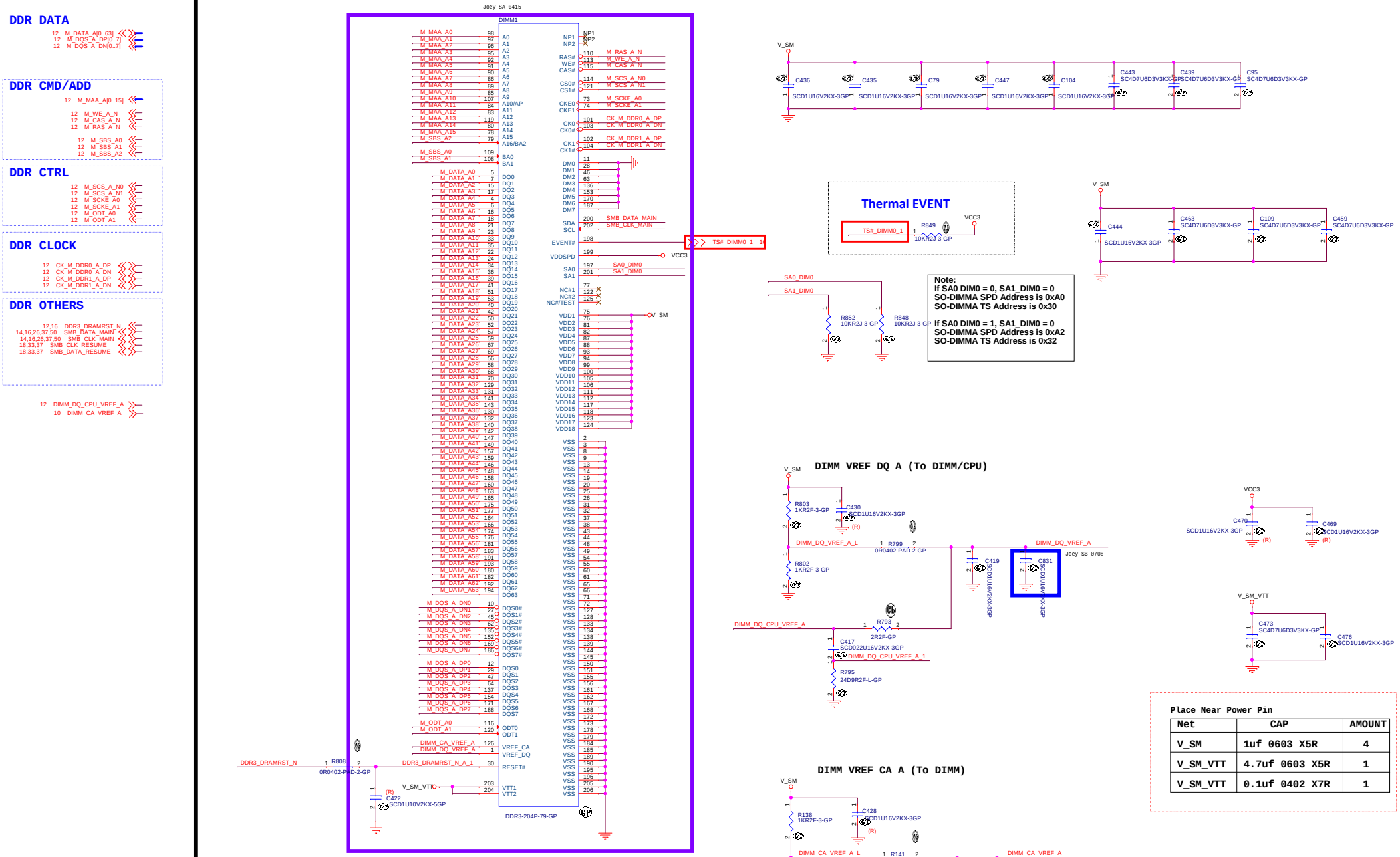
DDR DATA
12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]
DDR CMD/ADD
12 M_MAA_A[0..15]
12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2
DDR CTRL
12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1
DDR CLOCK
12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN
DDR OTHERS
12,16 DDR3_DRAMRST_N
14,16,26,37,50 SMB_DATA_MAIN
14,16,26,37,50 SMB_CLK_MAIN
18,33,37 SMB_CLK_RESUME
18,33,37 SMB_DATA_RESUME
12 DIMM_DQ_CPU_VREF_A
10 DIMM_CA_VREF_A
Joey_SA_8415
DIMM1
DDR3-204P-79-GP
DDR3_DRAMRST_N
R808
0R0402-PAD-2-GP
C422
SCD1U10V2KX-5GP
V_SM_VTT
TS#_DIMM0_1
VCC3
SMB_DATA_MAIN
SMB_CLK_MAIN
SA0_DIM0
SA1_DIM0
V_SM
Thermal EVENT
TS#_DIMM0_1
R849
10KR2J-3-GP
VCC3
C436
C435
C79
C447
C104
C443
SC4D7U6D3V3KX-GP
C439
SC4D7U6D3V3KX-GP
C95
SC4D7U6D3V3KX-GP
SCD1U16V2KX-3GP
C444
C463
SC4D7U6D3V3KX-GP
C109
SC4D7U6D3V3KX-GP
C459
SC4D7U6D3V3KX-GP
R852
10KR2J-3-GP
R848
10KR2J-3-GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
DIMM VREF DQ A (To DIMM/CPU)
R803
1KR2F-3-GP
C430
SCD1U16V2KX-3GP
DIMM_DQ_VREF_A_L
R799
0R0402-PAD-2-GP
DIMM_DQ_VREF_A
Joey_SB_0708
C419
C831
R802
1KR2F-3-GP
DIMM_DQ_CPU_VREF_A
R793
2R2F-GP
C417
SCD022U16V2KX-3GP
DIMM_DQ_CPU_VREF_A_1
R795
24D9R2F-L-GP
C470
C469
SCD1U16V2KX-3GP
V_SM_VTT
C473
SC4D7U6D3V3KX-GP
C476
SCD1U16V2KX-3GP
Place Near Power Pin
Net | CAP | AMOUNT
V_SM | 1uf 0603 X5R | 4
V_SM_VTT | 4.7uf 0603 X5R | 1
V_SM_VTT | 0.1uf 0402 X7R | 1
DIMM VREF CA A (To DIMM)
R138
1KR2F-3-GP
C428
SCD1U16V2KX-3GP
DIMM_CA_VREF_A_L
R141
0R0402-PAD-2-GP
DIMM_CA_VREF_A
Joey_SB_0708
R139
1KR2F-3-GP
C110
C832
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title DIMM_A
Size Custom
Document Number Rosa_Tigris AIO
Rev 1
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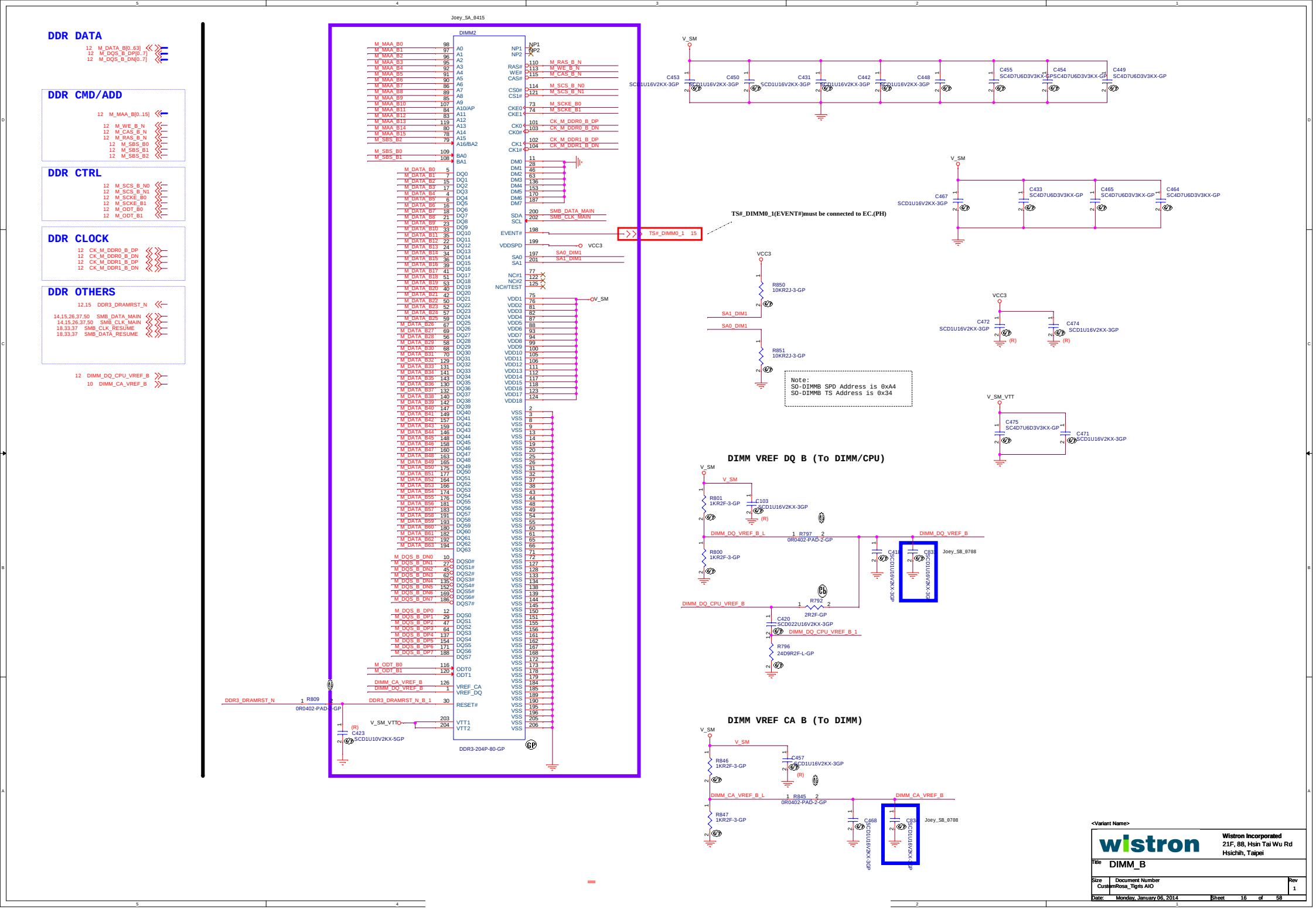
DDR DATA
12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]
DDR CMD/ADD
12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2
DDR CTRL
12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1
DDR CLOCK
12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN
DDR OTHERS
12,15 DDR3_DRAMRST_N
14,15,26,37,50 SMB_DATA_MAIN
14,15,26,37,50 SMB_CLK_MAIN
18,33,37 SMB_CLK_RESUME
18,33,37 SMB_DATA_RESUME
12 DIMM_DQ_CPU_VREF_B
10 DIMM_CA_VREF_B
Joey_SA_0415
DIMM2
DDR3-204P-80-GP
TS#_DIMM0_1 15
TS#_DIMM0_1(EVENT#)must be connected to EC.(PH)
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
DIMM VREF DQ B (To DIMM/CPU)
DIMM VREF CA B (To DIMM)
Joey_SB_0708
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title DIMM_B
Size Document Number Rev
CustomRosa_Tigris AIO 1
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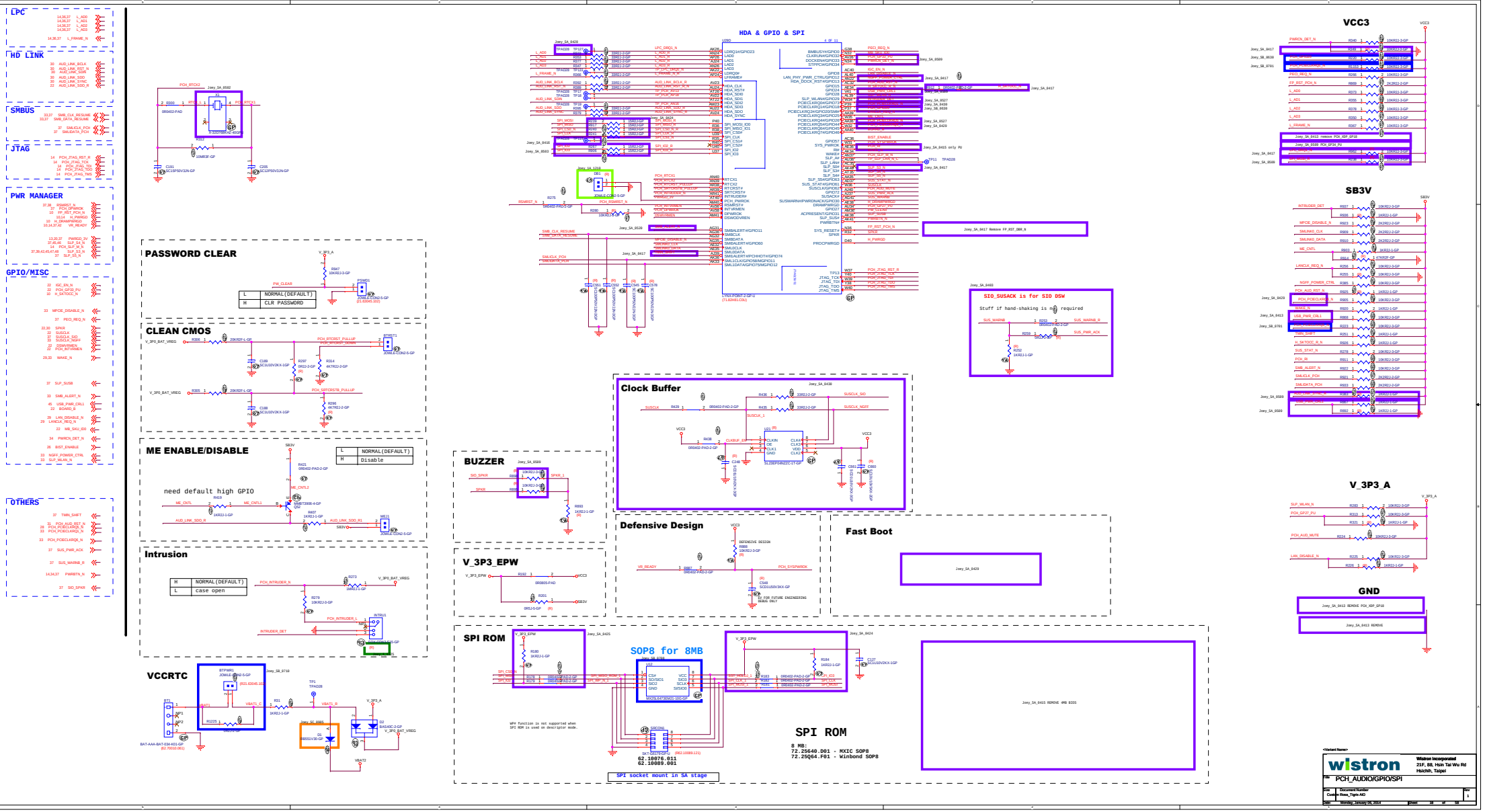
Remove Channel B, DIMM1


LPC
HD LINK
SMBUS
JTAG
PWR MANAGER
GPIO/MISC
OTHERS
HDA & GPIO & SPI
VCC3
SB3V
V_3P3_A
GND
PASSWORD CLEAR
CLEAN CMOS
ME ENABLE/DISABLE
need default high GPIO
Intrusion
VCCRTC
BUZZER
V_3P3_EPW
Clock Buffer
Defensive Design
Fast Boot
SPI ROM
SOP8 for 8MB
SPI ROM
8 MB:
72.25640.D01 - MXIC SOP8
72.25Q64.F01 - Winbond SOP8
62.10076.011
62.10089.001
SPI socket mount in SA stage
SIO_SUSACK is for SIO DSW
Stuff if hand-shaking is not required
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
PCH_AUDIO/GPIO/SPI
Monday, January 06, 2014

## CPU CLOCK

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

## PCI CLOCK

36 CK_P_33M_TPM
14 CK_P_33M_LPCP80
21 CK_PCH_33M_FB
37 CK_P_33M_SIO

## PCIE CLOCK

10 CK_DPNS_R_DN
10 CK_DPNS_R_DP

10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP

11 CK_DP_DN
11 CK_DP_DP

49 CK_PE_100M_16PORT_DP
49 CK_PE_100M_16PORT_DN

33 CLKOUT_PCIE0N
33 CLKOUT_PCIE0P

33 CLKOUT_PCIE1N
33 CLKOUT_PCIE1P

29 CK_GLAN_DN
29 CK_GLAN_DP

28 CLKOUT_PCIE4N
28 CLKOUT_PCIE4P

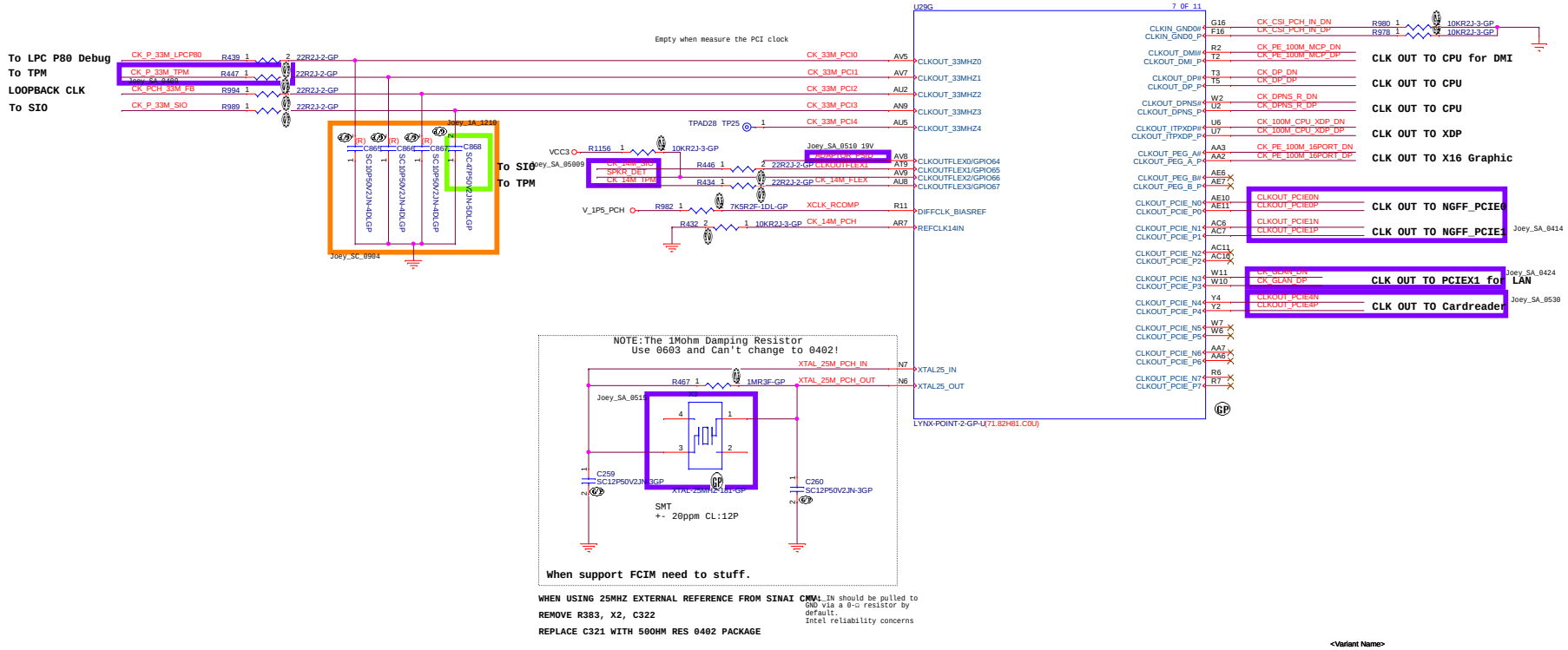
## 48M CLOCK

## 14M CLOCK

37 CK_14M_SIO
36 CK_14M_TPM

## Other

39 ADAPTOR_PSID
39 SPKR_DET




<Variant Name>

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Hsichih, Taipei

Title: PCH_CLK

Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1

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## MINI CARD

33 CLINK_CLK_LAN
33 CLINK_DATA_LAN
33 CLINK_RST_LAN_N

## DP PORT B

33 DDPB_AUX_DN
33 DDPB_AUX_DP
33 DDSP_B_HPD

## DP PORT D

26 DPD_AUXP
26 DPD_AUXN
26 DPD_HPD

21,25 PANEL_SEL1_CABLE_PCH

25 PANEL_SEL3_CABLE_PCH

34 OSD_DN
32 WEBCAM_DET

21,32 TP_DET

25 LVDS_DET_A*

25 LVDS_DET_B*

25 INV_DET*

22 BOARD_A

22 BOARD_C

22 MB_SKU_ID2

26 SMBUS_ISP

34 OSD_MENU

26 PCH_LVDS_BL_ADJ

## VGA

24 VGA_HSYNC_3V
24 VGA_VSYNC_3V
24 VGA_RED
24 VGA_GREEN
24 VGA_BLUE
24 VGA_PCH_DDCSDA
24 VGA_PCH_DDCSCL

## SATA

34 SATAHDR_RX_DN0
34 SATAHDR_RX_DP0
34 SATAHDR_TX_DN0
34 SATAHDR_TX_DP0

34 SATAHDR_RX_DN5
34 SATAHDR_RX_DP5
34 SATAHDR_TX_DN5
34 SATAHDR_TX_DP5

34 PCH_SATA_LED_N

## OTHERS

10 H_PM_SYNC_0
10 CPU_THERMTRIP_N
52 H_THERMTRIP_N

10,37 H_PECI
13,18,37 PWRGD_3V

37 A20GATE
37 KBRST_N
36,37 SER_IRQ

10,14 PLTRST_CPU_N
18,22,30 SPKR

## Straps

22 SATA1GP

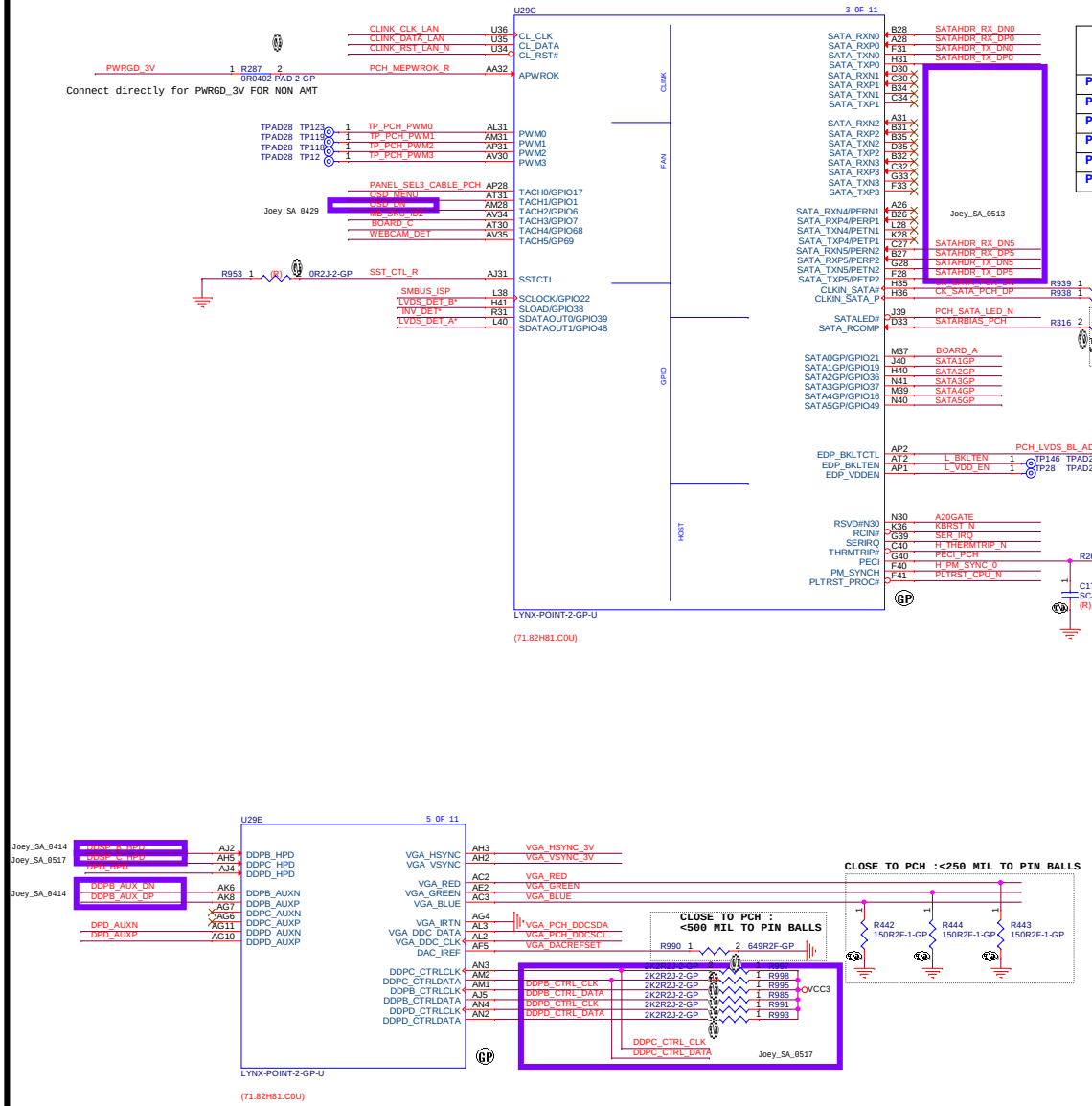
22 SATA2GP

22 SATA3GP

## HDMI

24 DDPC_CTRL_CLK
24 DDPC_CTRL_DATA

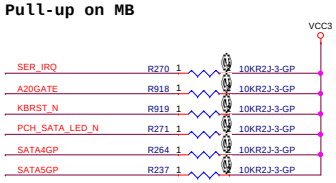
24 DDSP_C_HPD




## SATAS Port (H81)

| | SATA 3.0 PORT | SATA 2.0 Port |
|---|---|---|
| PORT0 | Support | Support |
| PORT1 | Support | Support |
| PORT2 | | Disabled |
| PORT3 | | Disabled |
| PORT4 | | Support |
| PORT5 | | Support |

## Pull-up on MB




| Soft strap | GPIO16 |
|---|---|
| 0 | SATA 4 |
| 1 | PCIe 1 |

Joey_SA_8417 Remove H_THERMTRIP_N PU

Joey_SA_8425

To configure I/O Port Flexibility via soft strap, set setting to 11b

Note: GPIO strap option is only available for SATA/PCIe muxed signals to support mSATA/mini PCIe port switching

| | |
|---|---|
| 00b | SATA |
| 01b | PCIe |
| 10b | Reserved |
| 11b | Setting based on GPIO<br>0 - SATA<br>1 - PCIe |


<Variant Name>

wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title PCH_SATA/FAN/DP/VGA

Size Custom | Document Number Rosa_Tigris AIO | Rev 1

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## DMI

11 DMI_MT_IR_DN[0..3]
11 DMI_MT_IR_DP[0..3]
11 DMI_IT_MR_DN[0..3]
11 DMI_IT_MR_DP[0..3]

## PCIE

33 HSI_DN2
33 HSI_DP2
33 HSO_C_DN2
33 HSO_C_DP2

33 HSI_DN3
33 HSI_DP3
33 HSO_C_DN3
33 HSO_C_DP3

29 HSI_LAN_DN4
29 HSI_LAN_DP4
29 HSO_C_LAN_DN4
29 HSO_C_LAN_DP4

28 HSI_DN5
28 HSI_DP5
28 HSO_C_DN5
28 HSO_C_DP5

## USB

27 USB_PCH_DN0
27 USB_PCH_DP0
27 USB_PCH_DN1
27 USB_PCH_DP1

32 USB_PCH_DN3
32 USB_PCH_DP3

32 USB_PCH_DN4
32 USB_PCH_DP4
33 USB_PCH_DN5
33 USB_PCH_DP5

27 USB_PCH_DN8
27 USB_PCH_DP8

27 USB_PCH_DN9
27 USB_PCH_DP9

27 USB_PCH_DN10
27 USB_PCH_DP10
27 USB_PCH_DN11
27 USB_PCH_DP11

21,27 USBOC01*
21,27 USBOC89*
21,27 USBOC1011*

## USB3.0

27 USB3_TX1_C_DN
27 USB3_TX1_C_DP
27 USB3_TX2_C_DN
27 USB3_TX2_C_DP

27 USB3_RX1_DN
27 USB3_RX1_DP
27 USB3_RX2_DN
27 USB3_RX2_DP

21,27 USBOC01*
21,27 USBOC89*
21,27 USBOC1011*

## FDI

11 FDI_TX_DN[0..1]
11 FDI_TX_DP[0..1]

11 FDI_INT
11 FDI_CSYNC

## OTHERS

37IO_SMI_N
19 CK_PCH_33M_FB
10,37 PLTRST_N

22 MB_SKU_ID1
25 PANEL_SEL1_CABLE_PCH
32 TP_DET

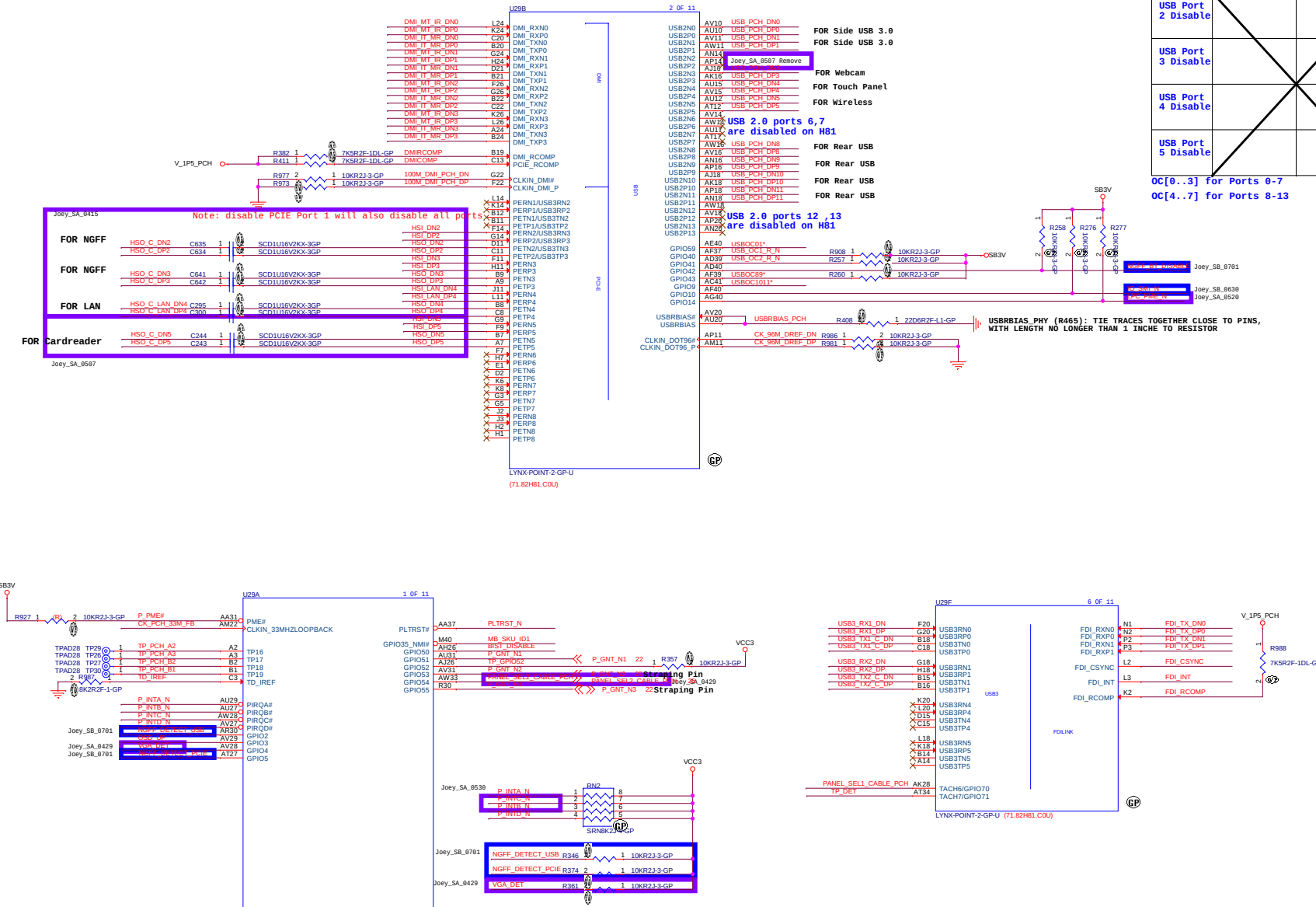
34 OSD_UP
24 VGA_DET
37 LPC_PME_N

19 NGFF_DETECT_USB
19 NGFF_DETECT_PCIE
NGFF_BT_DISABLE
26 BIST_DISABLE

## USB3.0 Port Mapping (H81)

| | USB 2.0 Signals | SuperSpeed Signals |
|---|---|---|
| USB Port 0 Enable | USBP0P<br>USBP0N | USB3Tp0<br>USB3Tn0<br>USB3Rn0<br>USB3Rp0 |
| USB Port 1 Enable | USBP1P<br>USBP1N | USB3Tp1<br>USB3Tn1<br>USB3Rn1<br>USB3Rp1 |
| USB Port 2 Disable | | |
| USB Port 3 Disable | | |
| USB Port 4 Disable | | |
| USB Port 5 Disable | | |

OC[0..3] for Ports 0-7
OC[4..7] for Ports 8-13





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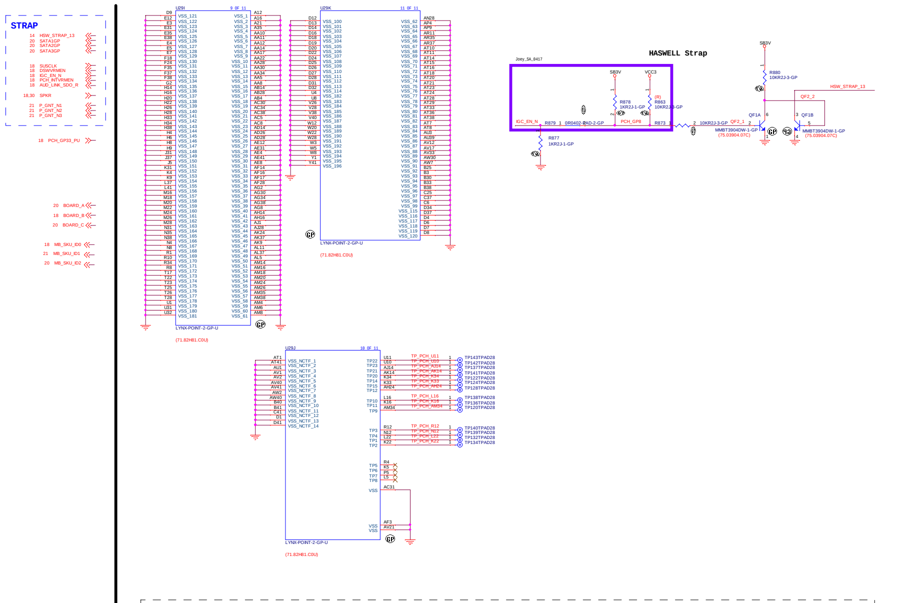
<Variant Name>

Title: PCH_FDI/PCIE/DMI/USB

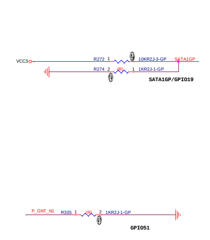
| Size | Document Number | Rev |
|---|---|---|
| Custom | Rosa_Tigris AIO | 1 |

Date: Monday, January 06, 2014 Sheet 21 of 58




| Board ID | | | |
|---|---|---|---|
| TYPE | ID2(GPIO21) | ID1(GPIO46) | ID0(GPIO68) |
| PRE SSI | 0 | 0 | 0 |
| SSI | 0 | 0 | 1 |
| PT | 0 | 1 | 0 |
| ST | 0 | 1 | 1 |
| A00 | 1 | 0 | 0 |
| A01 | 1 | 0 | 1 |
| A02 | 1 | 1 | 0 |
| A03 | 1 | 1 | 1 |

| SKU ID | | | |
|---|---|---|---|
| TYPE | ID2(GPIO7) | ID1(GPIO35) | ID0(GPIO32) |
| Tigris AIO UMA W/Touch | 0 | 0 | 0 |
| Tigris AIO UMA W/O Touch | 0 | 0 | 1 |
| Tigris AIO GPU W/Touch | 0 | 1 | 0 |
| Tigris AIO GPU W/O Touch | 0 | 1 | 1 |
| Caspian UMA W/Touch | 1 | 0 | 0 |
| Caspian UMA W/O Touch | 1 | 0 | 1 |
| Caspian GPU W/Touch | 1 | 1 | 0 |
| Caspian GPU W/O Touch | 1 | 1 | 1 |




## BOOT SELECT STRAPS

| BOOT DEVICE | GNT1/ GPIO51 | SATA1GP /GPIO19 |
|---|---|---|
| LPC | 0 | |
| SPI | 1 | |

DESIGN NOTE:
WEAK INTERNAL PULLUPS ON GP51. DEFAULT SPI BOOT DEVICE.

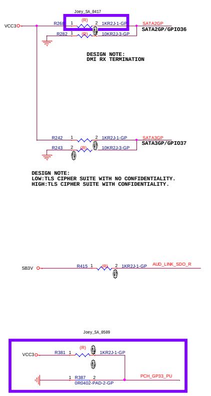



**Table 2-17. Functional Strap Definitions (Sheet 1 of 6)**

| Signal | Usage | When Sampled | Comment |
|---|---|---|---|
| SATA1GP / GPIO19 | Boot BIOS Strap bit 0 (BBS0) | Rising edge of PWROK | This signal has a weak internal pull-up.<br><br>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.<br><br>**Bit11 / Bit 10 / Boot BIOS Destination**<br>0 / 1 / Reserved<br>1 / 0 / Reserved<br>1 / 1 / SPI (default)<br>0 / 0 / LPC<br><br>**NOTES:**<br>1. The internal pull-up is disabled after PLTRST# deasserts.<br>2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.<br>3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN.<br>4. See Chapter 10, "GCS—General Control and Status Register" for additional information.<br>5. This signal is in the Core well. |

**Table 2-17. Functional Strap Definitions (Sheet 2 of 6)**

| Signal | Usage | When Sampled | Comment |
|---|---|---|---|
| GPIO51 | Boot BIOS Strap bit 1 (BBS1) | Rising edge of PWROK | This signal has a weak internal pull-up.<br><br>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.<br><br>**Bit11 / Bit 10 / Boot BIOS Destination**<br>0 / 1 / Reserved<br>1 / 0 / Reserved<br>1 / 1 / SPI (default)<br>0 / 0 / LPC<br><br>**NOTES:**<br>1. The internal pull-up is disabled after PLTRST# deasserts.<br>2. If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.<br>3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN.<br>4. See Chapter 10, "GCS—General Control and Status Register" for additional information.<br>5. This signal is in the Core well. |
| SATA2GP / GPIO36 | DMI RX Termination | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>This signal only takes effect if DMI is configured in **AC-coupled** mode (server/workstation only).<br><br>**0** = DMI RX is terminated to VSS.<br>**1** = DMI RX is terminated to VCC/2.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. If DMI is operating in DC-coupled mode (e.g. Client applications), then DMI RX is terminated to VSS and the value of this strap is ignored by the PCH and does not take effect.<br>3. This signal is in the Core well. |

**Table 2-17. Functional Strap Definitions (Sheet 3 of 6)**

| Signal | Usage | When Sampled | Comment |
|---|---|---|---|
| SATA3GP / GPIO37 | TLS Confidentiality | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>**0 = Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).<br>**1 = Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. This signal is in the Core well. |
| HDA_SDO | Flash Descriptor Security Override | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>**0 = Enable** security measures defined in the Flash Descriptor.<br>**1 = Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. Asserting HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.<br>3. This signal is in the Suspend well. |
| HDA_DOCK_EN# / GPIO33 | DMI TX Termination | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>This signal only takes effect if DMI is configured in **DC-coupled** mode.<br><br>**0** = DMI TX is terminated to VSS.<br>**1** = DMI TX is terminated to VCC/2.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. If DMI is operating in AC-coupled mode, then DMI TX is terminated to VCC/2 and the value of this strap does not take effect.<br>3. This signal is in the Core well. |

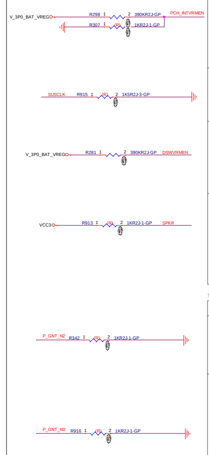



**Table 2-17. Functional Strap Definitions (Sheet 4 of 6)**

| Signal | Usage | When Sampled | Comment |
|---|---|---|---|
| INTVRMEN | Integrated VRM Enable | Always | This signal does not have an internal resistor; an **external** resistor is **required**.<br><br>**0** = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only; Desktop/Server/Workstation should not pull the strap low.<br>**1** = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.<br><br>**NOTES:**<br>1. This signal is always sampled.<br>2. This signal is in the RTC well. |
| GPIO62 / SUSCLK | PLL On-Die Voltage Regulator Enable | Rising edge of RSMRST# | This signal has a weak internal pull-up.<br><br>**0 = Disable** PLL On-Die voltage regulator.<br>**1 = Enable** PLL On-Die voltage regulator.<br><br>**NOTES:**<br>1. The internal pull-up is disabled after RSMRST# deasserts.<br>2. This signal is in the Suspend well. |
| DSWVRMEN | DeepSx Well On-Die Voltage Regulator Enable | Always | This signal does not have an internal resistor; an **external** resistor is **required**.<br><br>**0 = Disable** Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments.<br>**1 = Enable** DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.<br><br>**NOTES:**<br>1. This signal is always sampled.<br>2. This signal is in the RTC well. |
| SPKR | No Reboot | Rising edge of PWROK | The signal has a weak internal pull-down.<br><br>**0 = Disable** "No Reboot" mode.<br>**1 = Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: RCBA + Offset 3410h:Bit 5).<br>3. See Chapter 10, "GCS—General Control and Status Register" for additional information.<br>4. This signal is in the Core well. |

**Table 2-17. Functional Strap Definitions (Sheet 5 of 6)**

| Signal | Usage | When Sampled | Comment |
|---|---|---|---|
| GPIO53 | DMI AC-Coupling or DC-Coupling Mode | Rising edge of PWROK | This signal has a weak internal pull-up.<br><br>**0** = DMI is in **AC-coupling** mode (server/workstation only, not meant for desktop/mobile).<br>**1** = DMI is in **DC-coupling** mode (desktop, mobile or server/workstation).<br><br>**NOTES:**<br>1. The internal pull-up is disabled after PLTRST# deasserts.<br>2. This signal is in the Core well. |
| GPIO55 | Top Swap Override | Rising edge of PWROK | The signal has a weak internal pull-up.<br><br>**0 = Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate address lines (A16, A17, A18, A19 or A20) as selected in Top-Swap Block size soft strap (handled through FITc, also see Shark Bay SPI Flash Programming Guide CDI doc# 489495).<br>**1 = Disable** "Top Swap" mode.<br><br>**NOTES:**<br>1. The internal pull-up is disabled after PLTRST# deasserts.<br>2. Software will not be able to clear the Top Swap mode bit until the system is rebooted.<br>3. The status of this strap is readable using the Top Swap bit (Chipset Config Registers: RCBA + Offset 3414h:Bit 0).<br>4. This signal is in the Core well. |
| DDPB_CTRLDATA | Port B Detected | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>**0** = Port B is not detected.<br>**1** = Port B is detected.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. This signal is in the Core well. |
| DDPC_CTRLDATA | Port C Detected | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>**0** = Port C is not detected.<br>**1** = Port C is detected.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. This signal is in the Core well. |

**Table 2-17. Functional Strap Definitions (Sheet 6 of 6)**

| Signal | Usage | When Sampled | Comment |
|---|---|---|---|
| DDPD_CTRLDATA | Port D Detected | Rising edge of PWROK | This signal has a weak internal pull-down.<br><br>**0** = Port D is not detected.<br>**1** = Port D is detected.<br><br>**NOTES:**<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. This signal is in the Core well. |

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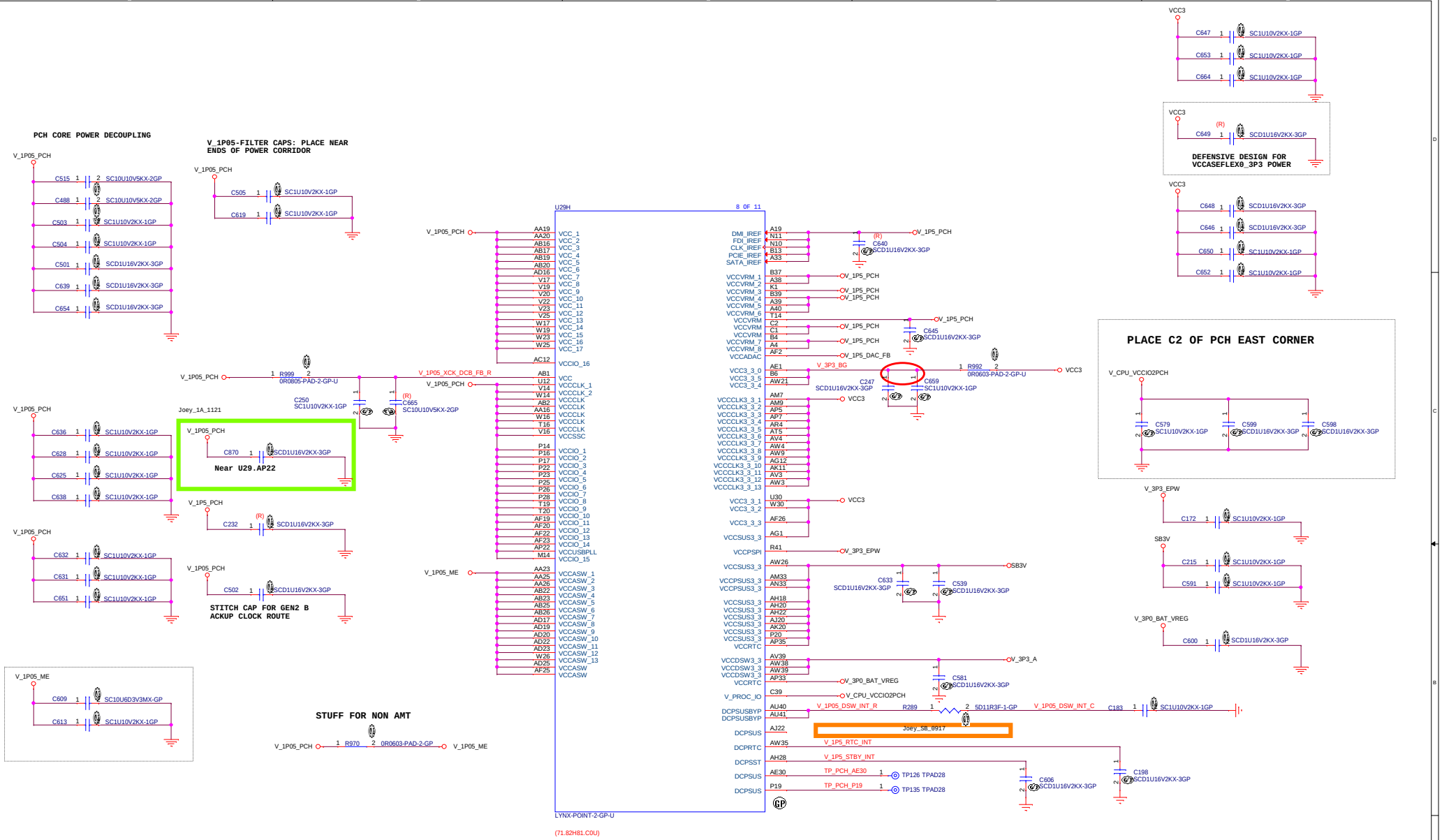
| | |
|---|---|
| Title | PCH_GND/STRAPS |
| Size | Custom |
| Document Number | Rosa_Tigris AIO |
| Rev | 1 |
| Date: | Monday, January 06, 2014 |
| Sheet | 22 of 58 |




| | | | |
|---|---|---|---|
| INTVRMEN | Integrated VRM Enable | Always | This signal does not have an internal resistor; an **external** resistor is **required.**<br><br>**0** = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only. Other systems should not pull the strap low.<br><br>**1** = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left floating.<br><br>**NOTES:**<br>1. This signal is always sampled.<br>2. This signal is in the RTC well. |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Title: PCH_POWER

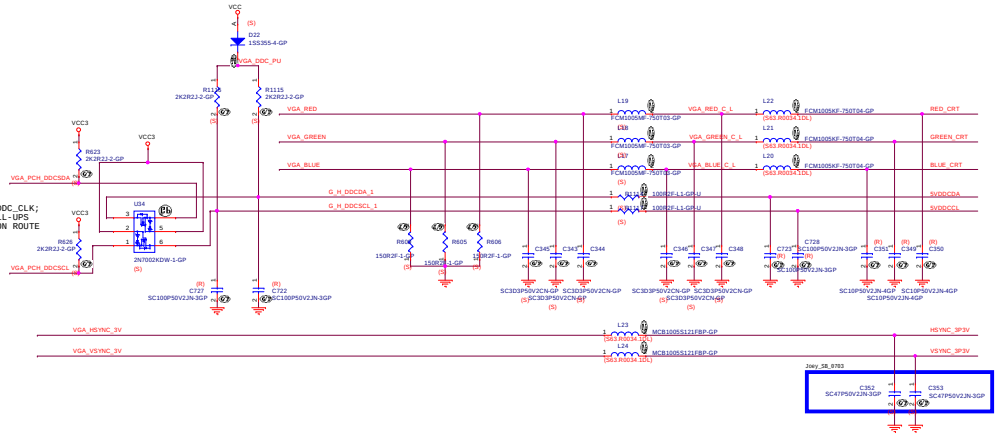
Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

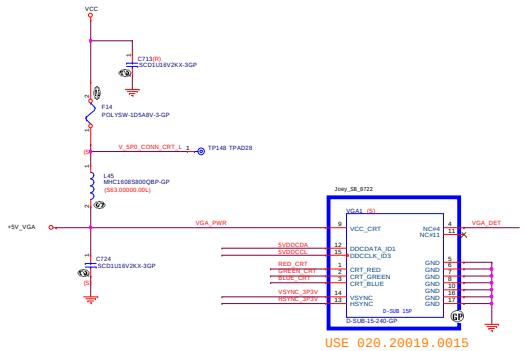
Date: Monday, January 06, 2014 | Sheet 23 of 58

## VGA

20 VGA_RED
20 VGA_GREEN
20 VGA_BLUE
20 VGA_HSYNC_3V
20 VGA_VSYNC_3V
20 VGA_PCH_DDCSDA
20 VGA_PCH_DDCSCL
21 VGA_DET

# VGA PORT

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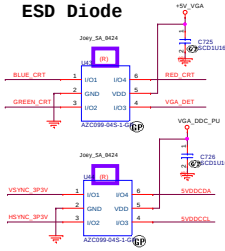
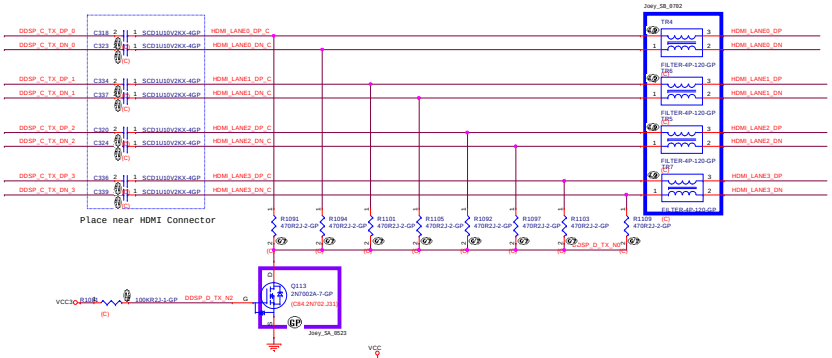
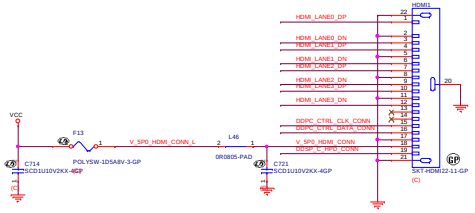


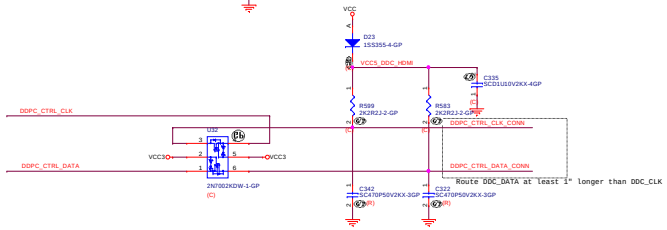

## HDMI

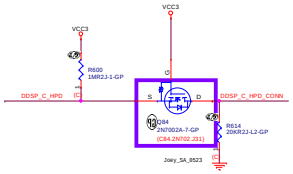
11 DDSP_C_TX_DP_0
11 DDSP_C_TX_DN_0
11 DDSP_C_TX_DP_1
11 DDSP_C_TX_DN_1
11 DDSP_C_TX_DP_2
11 DDSP_C_TX_DN_2
11 DDSP_C_TX_DP_3
11 DDSP_C_TX_DN_3
20 DDPC_CTRL_CLK
20 DDPC_CTRL_DATA
20 DDSP_C_HPD

# HDMI

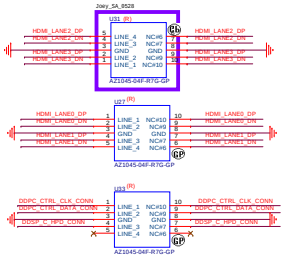



## ESD





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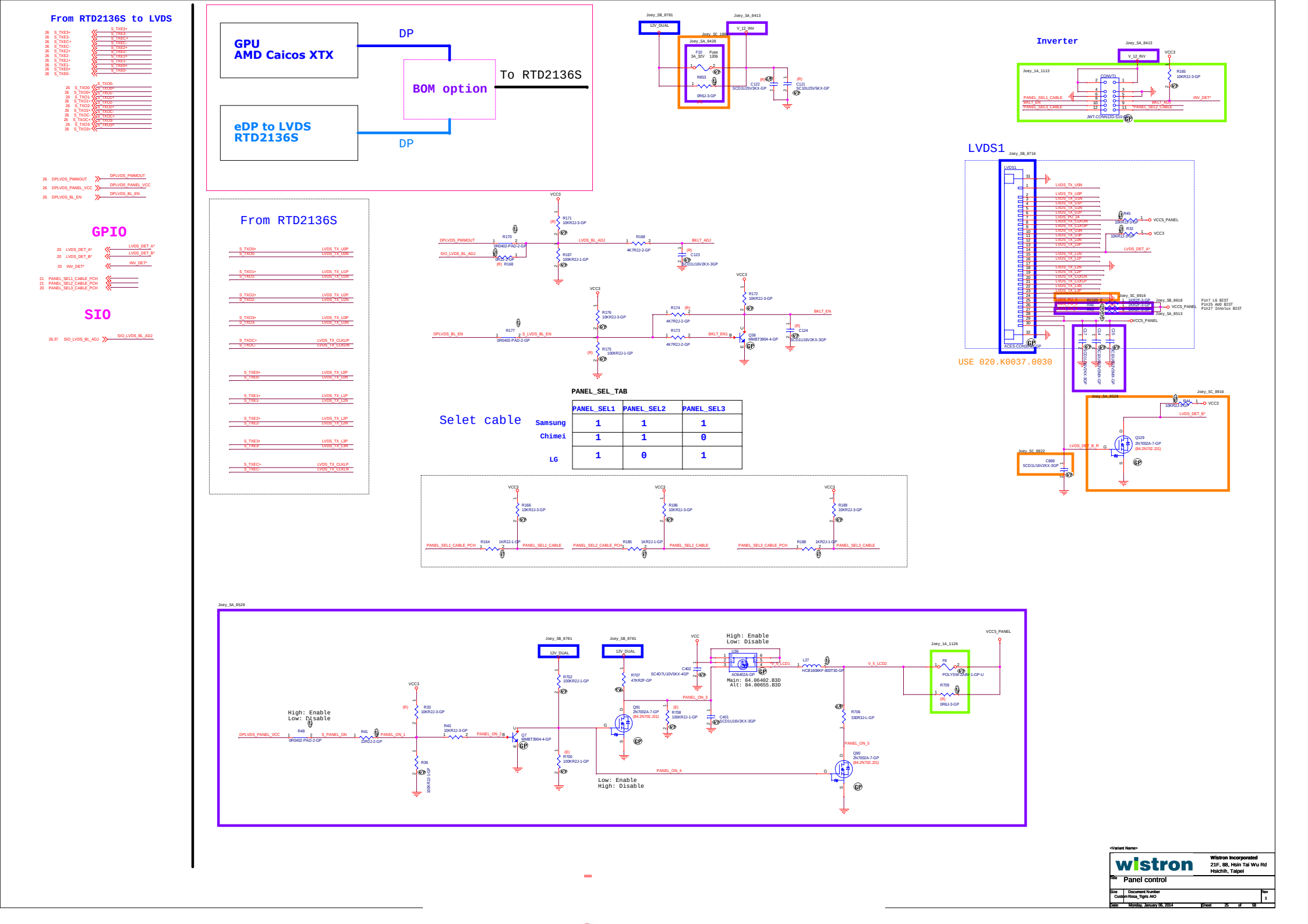
Title VGA/HDMI
Size D
Document Number Rosa_Tigris AIO
Rev SB
Date: Monday, January 06, 2014
Sheet 24 of 57


From RTD2136S to LVDS
GPU
AMD Caicos XTX
DP
BOM option
To RTD2136S
eDP to LVDS
RTD2136S
DP
Inverter
LVDS1
USE 020.K0037.0030
GPIO
SIO
From RTD2136S
Selet cable
PANEL_SEL_TAB
PANEL_SEL1 PANEL_SEL2 PANEL_SEL3
Samsung 1 1 1
Chimei 1 1 0
LG 1 0 1
High: Enable
Low: Disable
Main: 84.06402.B3D
Alt: 84.00655.B3D
Low: Enable
High: Disable
Panel control
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Hsichih, Taipei
Monday, January 06, 2014

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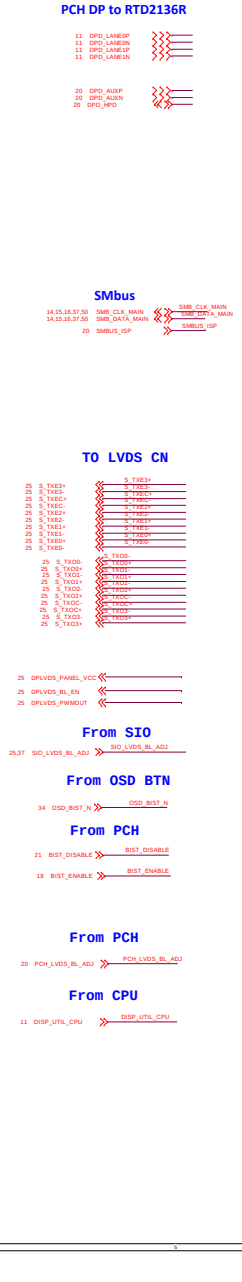
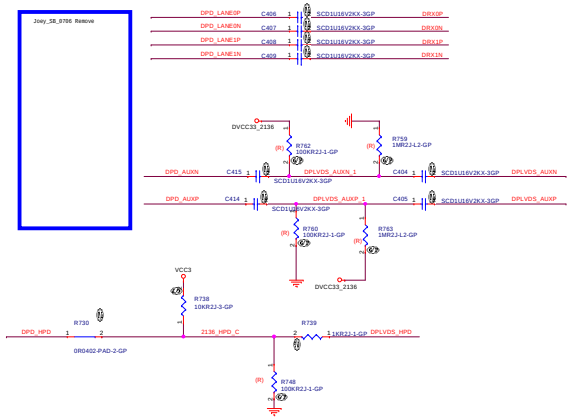
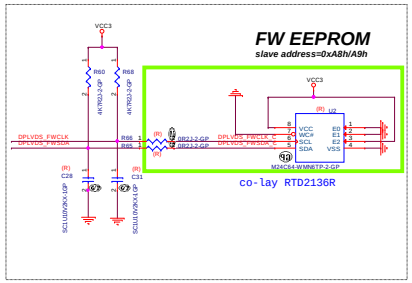
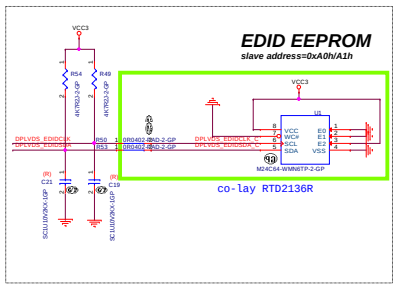
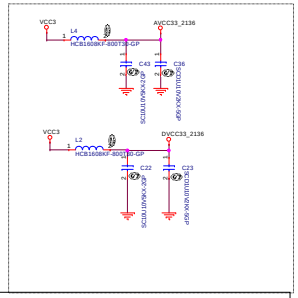
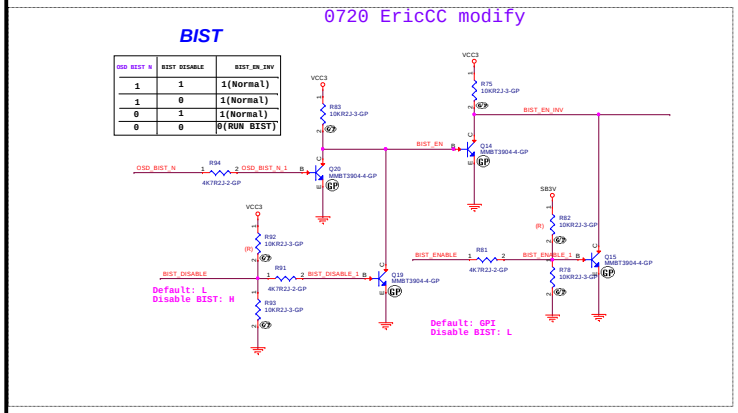


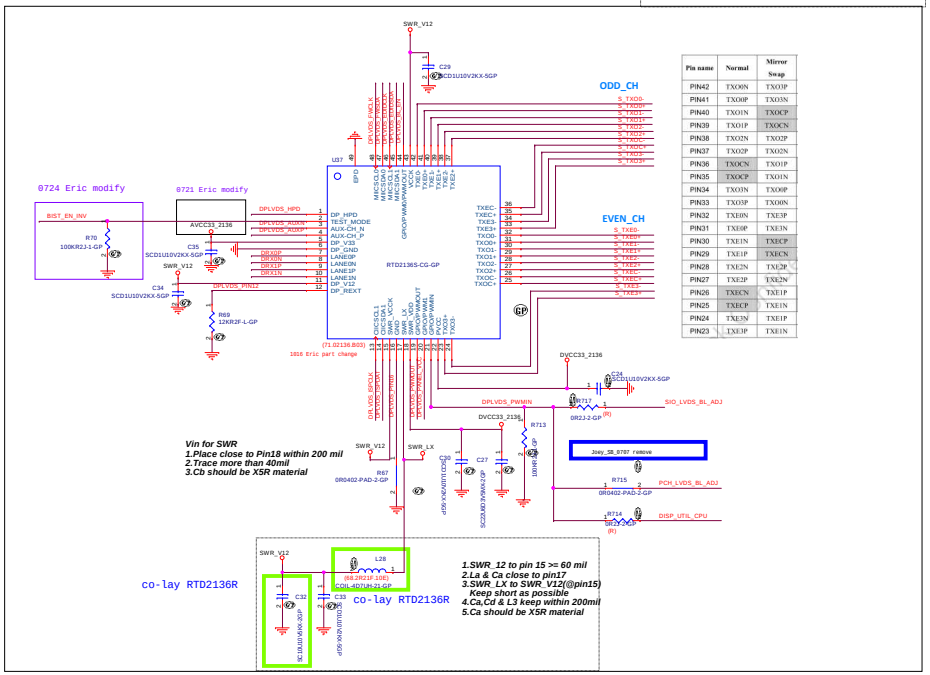



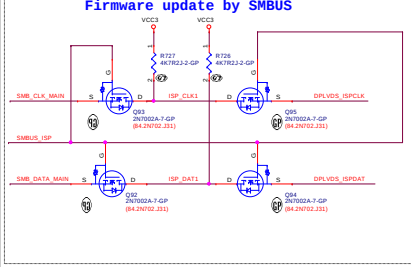



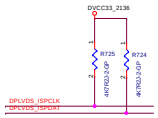



| OSD BIST N | BIST DISABLE | BIST_EN_INV |
|---|---|---|
| 1 | 1 | 1(Normal) |
| 1 | 0 | 1(Normal) |
| 0 | 1 | 1(Normal) |
| 0 | 0 | 0(RUN BIST) |




| Pin name | Normal | Mirror Swap |
|---|---|---|
| PIN42 | TXO0N | TXO3P |
| PIN41 | TXO0P | TXO3N |
| PIN40 | TXO1N | TXOCP |
| PIN39 | TXO1P | TXOCN |
| PIN38 | TXO2N | TXO2P |
| PIN37 | TXO2P | TXO2N |
| PIN36 | TXOCN | TXO1P |
| PIN35 | TXOCP | TXO1N |
| PIN34 | TXO3N | TXO0P |
| PIN33 | TXO3P | TXO0N |
| PIN32 | TXE0N | TXE3P |
| PIN31 | TXE0P | TXE3N |
| PIN30 | TXE1N | TXECP |
| PIN29 | TXE1P | TXECN |
| PIN28 | TXE2N | TXE2P |
| PIN27 | TXE2P | TXE2N |
| PIN26 | TXECN | TXE1P |
| PIN25 | TXECP | TXE1N |
| PIN24 | TXE3N | TXE0P |
| PIN23 | TXE3P | TXE0N |




co-lay RTD2136R notice
1. unmount: R591. R590. U23
   mount: R667. R666. U41
2. L47 change to 2.2uH(68.2R21F.10E)
3. C440 change to 10uF(78.10623.51L)

**Dual Mode Regulator Configuration**

| | 2.2-uH(L47) | 0 ohm(L47) |
|---|---|---|
| SWR | Connect | NC |
| LDO | NC | Connect |

**Mode Configure Table(Power On Latch)**

| | | MODE_CFG0(PIN47) | |
|---|---|---|---|
| | | 0 | 1 |
| MODE_CFG1(PIN48) | 0 | X | EP MODE |
| | 1 | ROM ONLY MODE | EEPROM MODE |


<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: DPtoLVDS_RTD2136R
Size: D | Document Number: Rosa_Tigris A/D | Rev: 1
Date: Monday, January 06, 2014 | Sheet 24 of 58

0717 modify

## USB

21 USB_PCH_DP0
21 USB_PCH_DN0
21 USB_PCH_DP1
21 USB_PCH_DN1
21 USBOC01*

21 USB_PCH_DP8
21 USB_PCH_DN8
21 USB_PCH_DP9
21 USB_PCH_DN9
21 USBOC89*

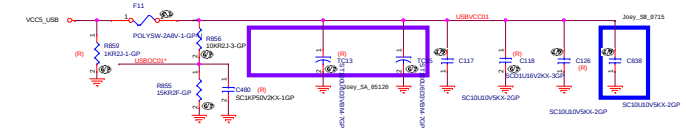
21 USB_PCH_DP10
21 USB_PCH_DN10
21 USB_PCH_DP11
21 USB_PCH_DN11
21 USBOC1011*

## USB 3.0

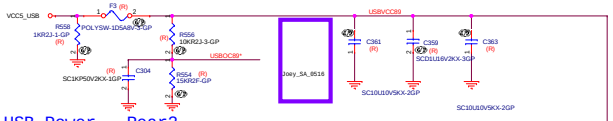
21 USB3_RX1_DN
21 USB3_RX1_DP
21 USB3_TX1_C_DN
21 USB3_TX1_C_DP

21 USB3_RX2_DN
21 USB3_RX2_DP
21 USB3_TX2_C_DN
21 USB3_TX2_C_DP

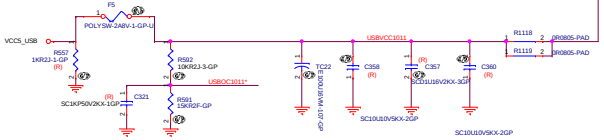
## USB_Power...Side1




## USB_Power...Rear1

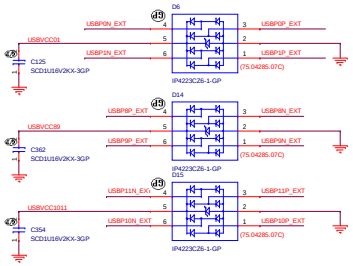


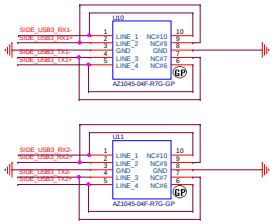

## USB_Power...Rear2




### EMI

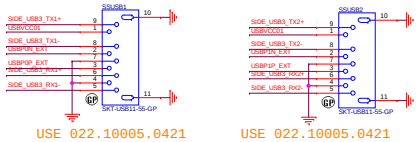
## ESD




Joey_SA_8425

## Side USB 3.0

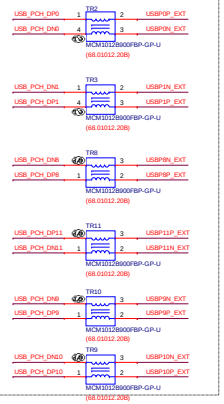


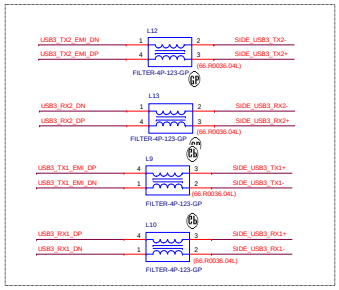

USE 022.10005.0421 USE 022.10005.0421

Joey_SA_8522

## Rear USB1

## Rear USB2




<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB/USB30

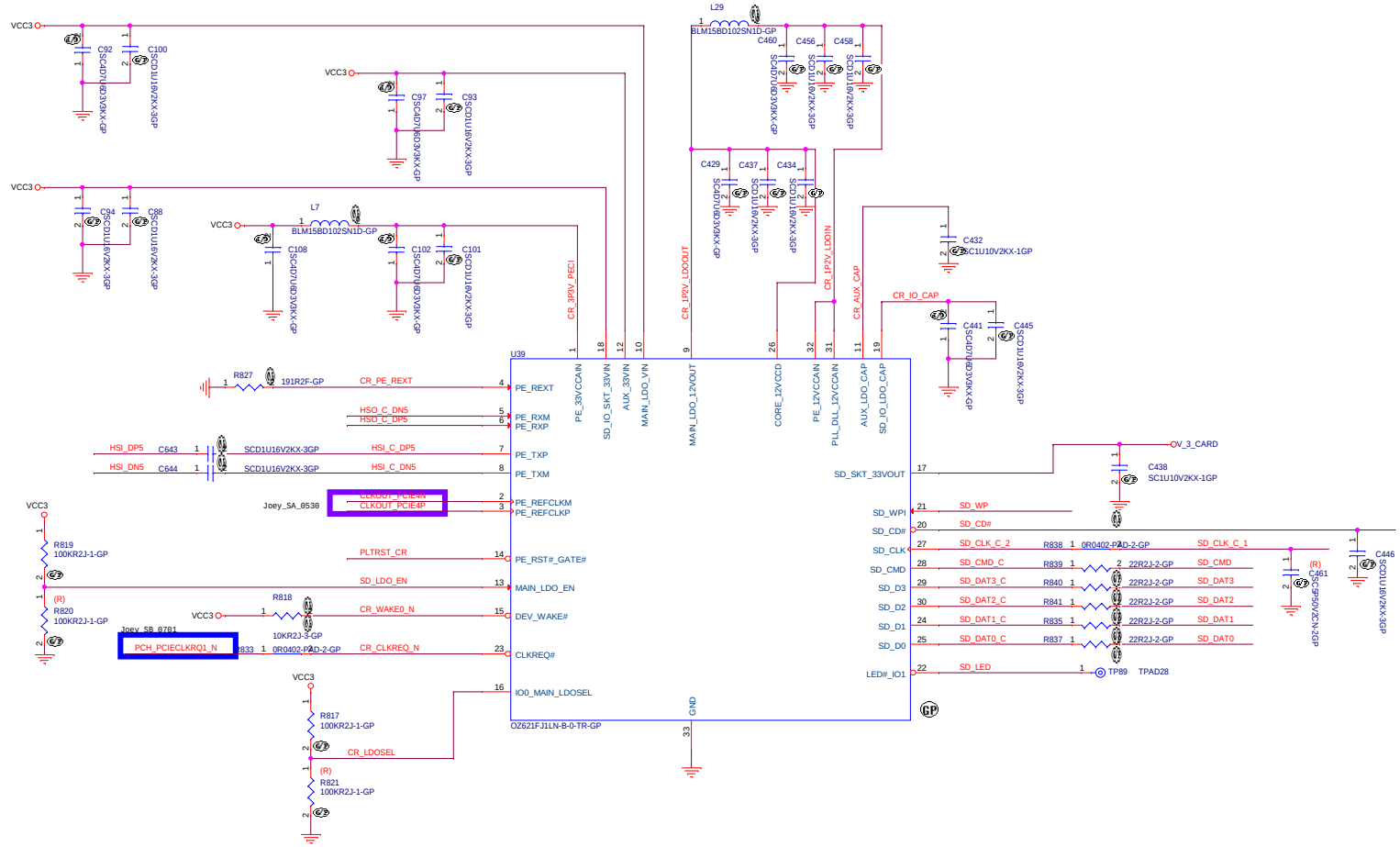
| Size | Document Number | Rev |
|---|---|---|
| Custom | Ross_Tigris AIO | 1 |

Date: Monday, January 06, 2014 Sheet 27 of 58

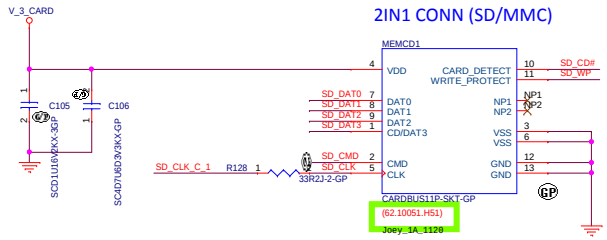
# Card Reader

21 HSI_DN5
21 HSI_DP5
21 HSO_C_DN5
21 HSO_C_DP5

19 CLKOUT_PCIE4N
19 CLKOUT_PCIE4P
18 PCH_PCIECLKRQ1_N
37 PLTRST_CR




## 2IN1 CONN (SD/MMC)




<Variant Name>

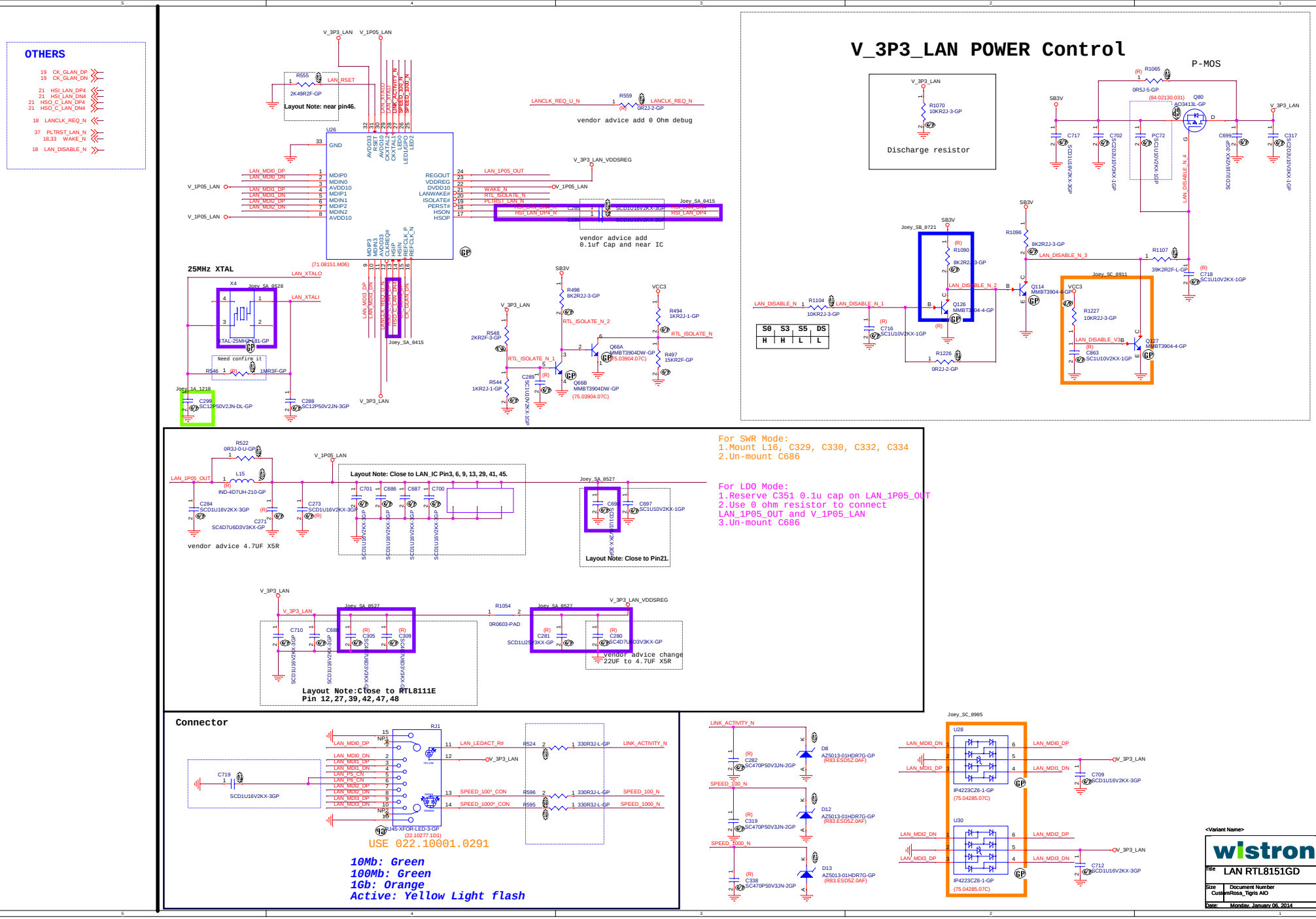
wistron

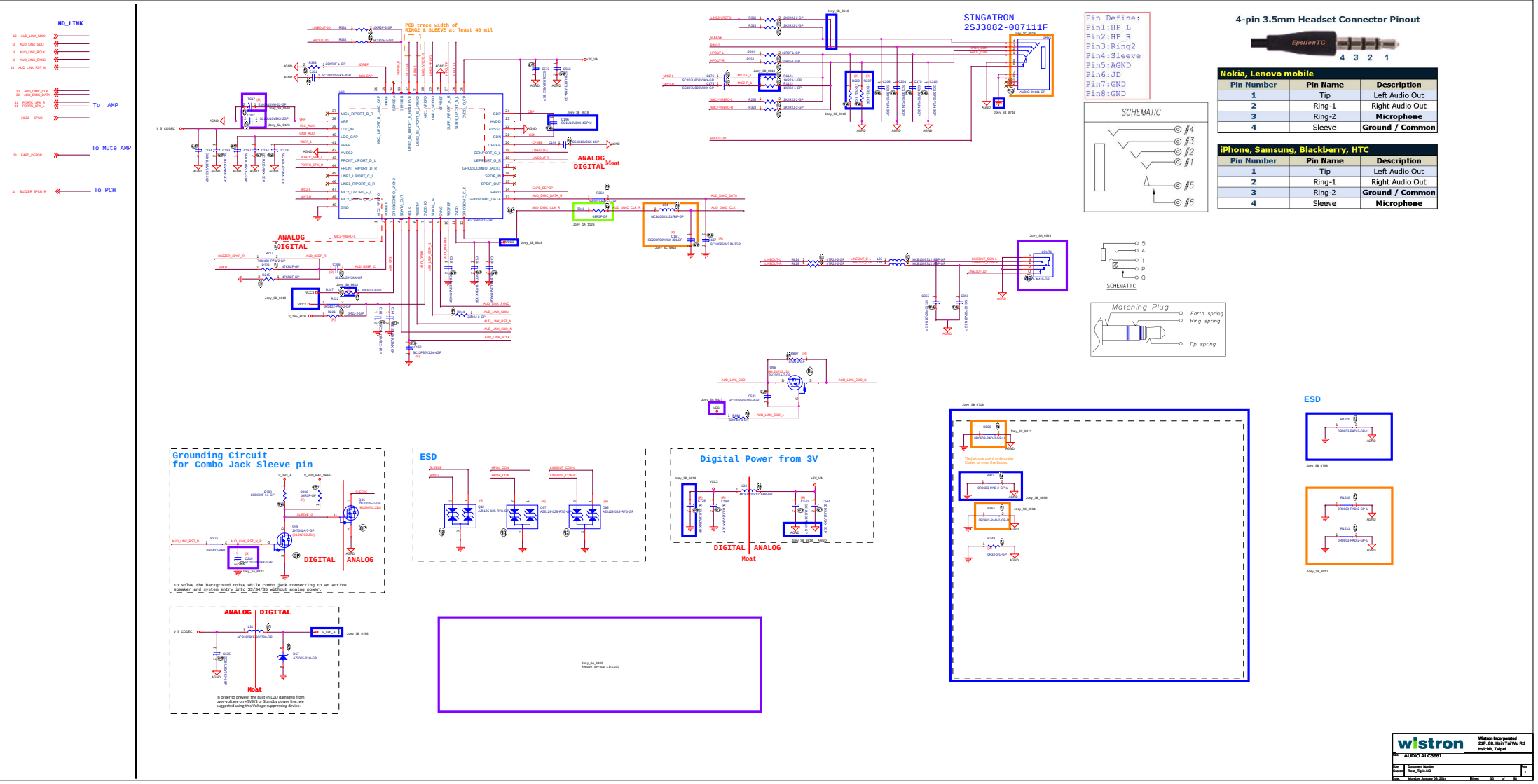
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Card Reader OZ621

| Size | Document Number | Rev |
|---|---|---|
| C | Rosa_Tigris AIO | 1 |

Date: Monday, January 06, 2014 Sheet 28 of 58


OTHERS
V_3P3_LAN POWER Control
P-MOS
Discharge resistor
25MHz XTAL
Layout Note: near pin46.
vendor advice add 0 Ohm debug
vendor advice add 0.1uf Cap and near IC
Layout Note: Close to LAN_IC Pin3, 6, 9, 13, 29, 41, 45.
Layout Note: Close to Pin21.
vendor advice 4.7UF X5R
Layout Note:Close to RTL8111E Pin 12,27,39,42,47,48
vendor advice change 22UF to 4.7UF X5R
For SWR Mode:
1.Mount L16, C329, C330, C332, C334
2.Un-mount C686
For LDO Mode:
1.Reserve C351 0.1u cap on LAN_1P05_OUT
2.Use 0 ohm resistor to connect LAN_1P05_OUT and V_1P05_LAN
3.Un-mount C686
Connector
USE 022.10001.0291
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
LAN RTL8151GD
Document Number
Rev 1
Monday, January 06, 2014
Sheet 29 of 58




## 4-pin 3.5mm Headset Connector Pinout




**Nokia, Lenovo mobile**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | Tip | Left Audio Out |
| 2 | Ring-1 | Right Audio Out |
| 3 | Ring-2 | Microphone |
| 4 | Sleeve | Ground / Common |

**iPhone, Samsung, Blackberry, HTC**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | Tip | Left Audio Out |
| 2 | Ring-1 | Right Audio Out |
| 3 | Ring-2 | Ground / Common |
| 4 | Sleeve | Microphone |

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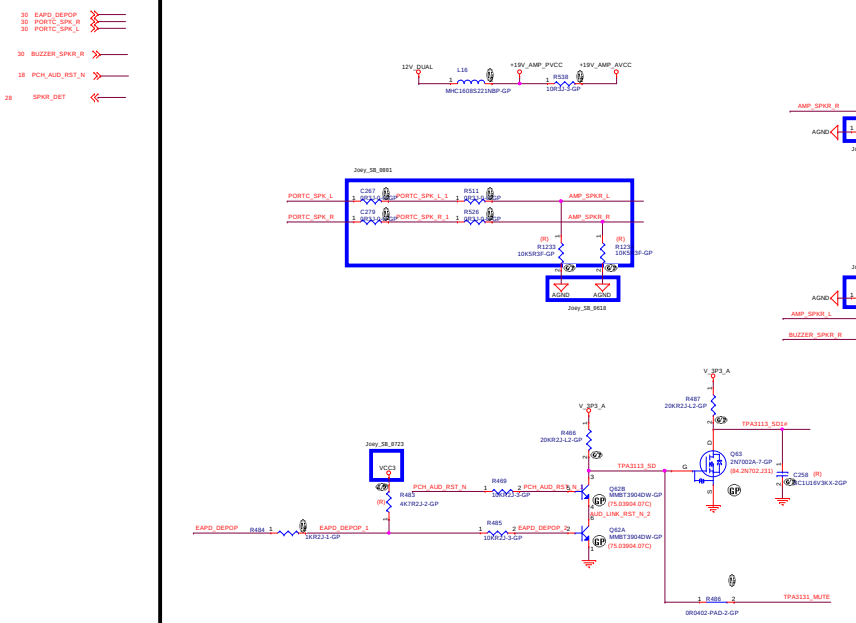
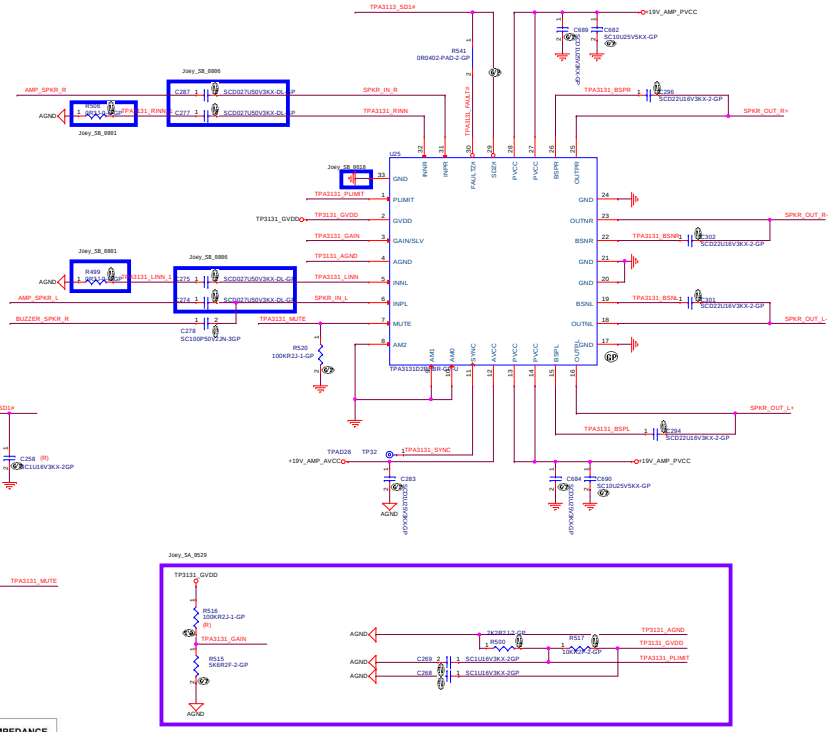
Hsichih, Taipei

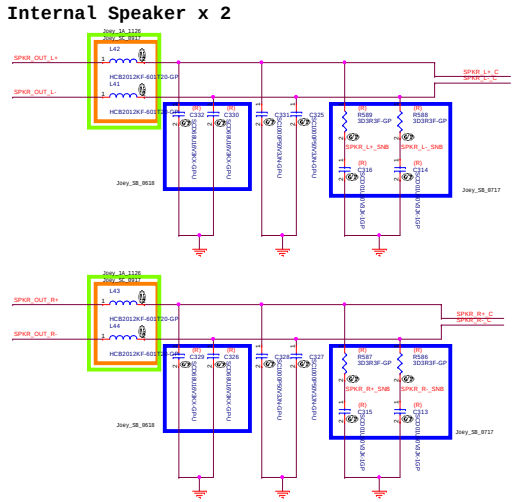
Title: AUDIO ALC3661

Size: Custom | Document Number: Rosa_Tigris.AIO | Rev: 1

Date: Monday, January 09, 2011 | Sheet 30 of 58







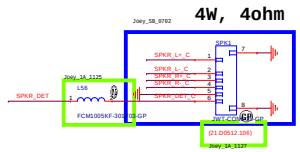




**Table 1. GAIN and MASTER/SLAVE**

| MASTER / SLAVE MODE | GAIN | R1 (to GND)(1) | R2 (to GVDD)(1) | INPUT IMPEDANCE |
|---|---|---|---|---|
| Master | 20 dB | 5.6 kΩ | OPEN | 60 kΩ |
| Master | 26 dB | 20 kΩ | 100 kΩ | 30 kΩ |
| Master | 32 dB | 39 kΩ | 100 kΩ | 15 kΩ |
| Master | 36 dB | 47 kΩ | 75 kΩ | 9 kΩ |
| Slave | 20 dB | 51 kΩ | 51 kΩ | 60 kΩ |
| Slave | 26 dB | 75 kΩ | 47 kΩ | 30 kΩ |
| Slave | 32 dB | 100 kΩ | 39 kΩ | 15 kΩ |
| Slave | 36 dB | 100 kΩ | 16 kΩ | 9 kΩ |

(1) Resistor tolerance should be 5% or better.

**Table 2. Recommended Input AC-Coupling Capacitors**

| GAIN | INPUT IMPEDANCE | INPUT CAPACITANCE | HIGH-PASS FILTER |
|---|---|---|---|
| 20 dB | 60 kΩ | 1.5 µF | 1.8 Hz |
| 26 dB | 30 kΩ | 3.3 µF | 1.6 Hz |
| 32 dB | 15 kΩ | 5.6 µF | 2.3 Hz |
| 36 dB | 9 kΩ | 10 µF | 1.8 Hz |

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \qquad (2)$$

Where:

$R_S$ is the total series resistance including $R_{DS(on)}$, and output filter resistance.
$R_L$ is the load resistance.
$V_P$ is the peak amplitude
$V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
$P_{OUT}$ (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

**Table 3. POWER LIMIT Example**

| $PV_{CC}$ (V) | PLIMIT VOLTAGE (V)(1) | R to GND | R to GVDD | OUTPUT VOLTAGE ($V_{rms}$) |
|---|---|---|---|---|
| 24 V | GVDD | Short | Open | 17.90 |
| 24 V | 3.3 | 45 kΩ | 51 kΩ | 12.67 |
| 24 V | 2.25 | 24 kΩ | 51 kΩ | 9.00 |
| 12 V | GVDD | Short | Open | 10.33 |
| 12 V | 2.25 | 24 kΩ | 51 kΩ | 9.00 |
| 12 V | 1.5 | 18 kΩ | 68 kΩ | 6.30 |

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to $1V_{rms}$.

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AMP TPA3131

Size: D | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 31 of 58

## WEBCAM

21 USB_PCH_DN3
21 USB_PCH_DP3
30 AUD_DMIC_CLK
30 AUD_DMIC_DATA

## USB TOUCH PANEL

21 USB_PCH_DN4
21 USB_PCH_DP4
21 TP_DET
20 WEBCAM_DET

Joey_SA_0423

## TOUCH PANEL

Joey_SA_0428
Joey_1A_1210
F4 POLYSW-1D5A8V-3-GP
VCC5_USB
R602 0R3J-0-U-GP
USBVCCTP
C333 SC10U10V5KX-2GP

Joey_1A_1120
Joey_SA_0428
Joey_SA_0513
12V_DUAL PR73 0R3J-0-U-GP
VCC12 PR72 0R3J-0-U-GP
TP_VCC12_C
F2 POLYSW-1D5A8V-3-GP
R486 0R3J-0-U-GP
TP_VCC12
C246 SC10U25V5KX-GP
Joey_SC_1001
TOUCH2
JWT-CON2-S14-GP-U

TR13
USB_PCH_DP4 USB_PCH_DP4_PP
USB_PCH_DN4 USB_PCH_DN4_NN
MCM1012B900FBP-GP-U
(T68.01012.20B)

FOR EMI
USB_PCH_DP4_PP
USB_PCH_DN4_NN
Joey_SB_0708
C708 SC10P50V2JN-4GP
C711 SC10P50V2JN-4GP

VCC3
R579 10KR2J-3-GP
TP_DET
USBVCCTP
TOUCH1
USB_PCH_DP4_PP
USB_PCH_DN4_NN
JWT-CON5-S13-GP

USE 021.60059.0105

## WEBCAM

TR1
USB_PCH_DP3 USB_PCH_DP3_PP
USB_PCH_DN3 USB_PCH_DN3_NN
MCM1012B900FBP-GP-U
(68.01012.20B)

FOR EMI
WEBCAM_DET
PC2 SC22P50V2JN-4GP

Joey_SC_1001
VCC3
F7 POLYSW-1D5A8V-3-GP
R705 0R3J-0-U-GP
VCC3_CAM
Joey_SC_0904
C840 SC10U10V5KX-2GP
C397 SC10U10V5KX-2GP
C396 SC10U16V2KX-3GP
SB3V
R703 0R3J-0-U-GP
F6 POLYSW-1D5A8V-3-GP

VCC3
R30 10KR2J-3-GP
WEBCAM_DET
VCC3_CAM
WEBCM1
USB_PCH_DP3_PP
USB_PCH_DN3_NN
AUD_DMIC_CLK
AUD_DMIC_DATA
JWT-CON8-4-GP
Joey_SB_0719

USE 021.F0001.0008

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Touch/Webcam

| Size | Document Number | Rev |
|---|---|---|
| C | Rosa_Tigris AIO | 1 |

Date: Monday, January 06, 2014 Sheet 32 of 58

## HDMI

11 DDSP_B_TX_DP_0
11 DDSP_B_TX_DN_0

11 DDSP_B_TX_DP_1
11 DDSP_B_TX_DN_1

11 DDSP_B_TX_DP_2
11 DDSP_B_TX_DN_2

11 DDSP_B_TX_DP_3
11 DDSP_B_TX_DN_3

20 DDSP_B_HPD

20 DDPB_AUX_DN
20 DDPB_AUX_DP

## CLINE

20 CLINK_CLK_LAN
20 CLINK_DATA_LAN
20 CLINK_RST_LAN_N

## PCIE

21 HSI_DN2
21 HSI_DP2
21 HSO_C_DN2
21 HSO_C_DP2

19 CLKOUT_PCIE0N
19 CLKOUT_PCIE0P

21 HSI_DN3
21 HSI_DP3
21 HSO_C_DN3
21 HSO_C_DP3

19 CLKOUT_PCIE1N
19 CLKOUT_PCIE1P

PCH 18 PCIECLKRQ5_N
PCH 18 PCIECLKRQ6_N

## USB

21 USB_PCH_DN5
21 USB_PCH_DP5

## I2C

18,37 SMB_CLK_RESUME
18,37 SMB_DATA_RESUME
18 SMB_ALERT_N

## CLOCK

18 SUSCLK_NGFF

## OTHER

18,29 WAKE_N
18 MPCIE_DISABLE_N
18 NGFF_BT_DISABLE
37 PCIE_RST#
18 NGFF_POWER_CTRL
18 SLP_WLAN_N
18,29 NGFF_DETECT_PCIE
18,29 NGFF_DETECT_USB

# NGFF(A Key)

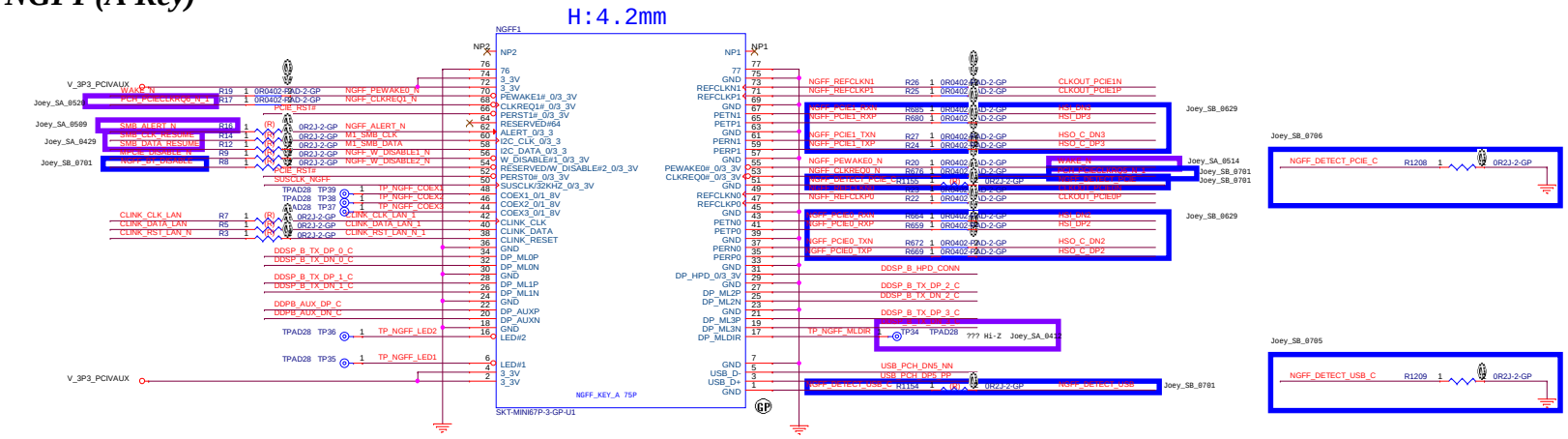
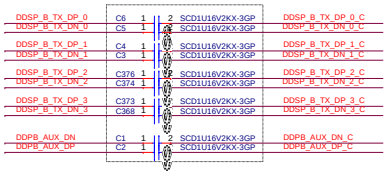


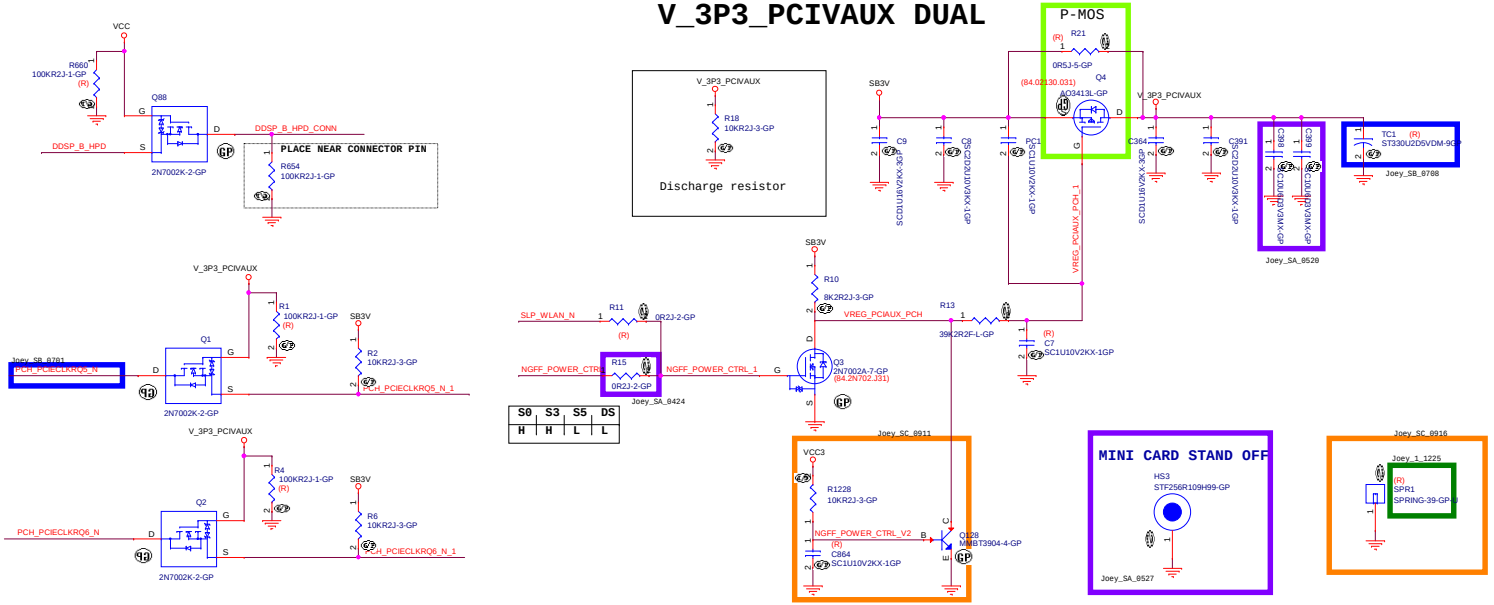

**Table 19. MLDIR Pin Termination**

| Display-Capability on Display-M.2 Card | Example | MLDIR Pin Termination on Display-M.2 Card |
|---|---|---|
| DisplayPort Sink | Card is a wireless display transmitter | Terminated directly to GND |
| DisplayPort Source | Card is a wireless display receiver | Terminated directly to +3.3V |
| DisplayPort Sink or Source | Card is configurable as either a wireless display transmitter or receiver | Hi-Z (single input load) |

**Place all CAP near DP Connector**




# V_3P3_PCIVAUX DUAL




<Variant Name>

wistron

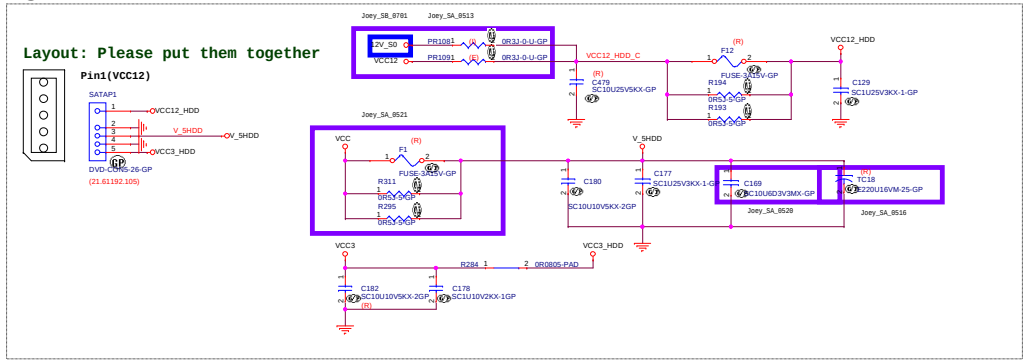
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

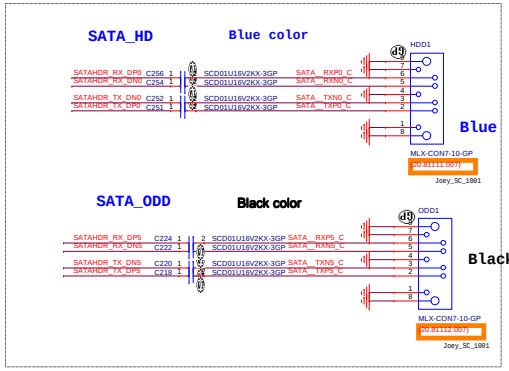
Title: NGFF

Size: Document Number: CusamRosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 33 of 58

# SATA




Use LOTES vendor

## SATA

20 SATAHDR_RX_DP0
20 SATAHDR_RX_DN0
20 SATAHDR_TX_DN0
20 SATAHDR_TX_DP0
20 SATAHDR_RX_DP5
20 SATAHDR_RX_DN5
20 SATAHDR_TX_DN5
20 SATAHDR_TX_DP5

## Power Botton/Reset

14,18,37 PWRBTN_N

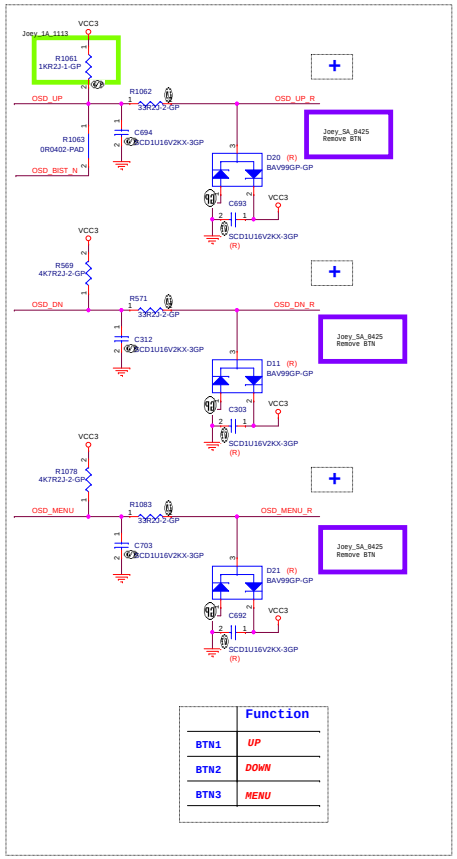
TO SIO

## HD_LED

20 PCH_SATA_LED_N
37 SIO_HDD_LED
37 SIO_YELLOW
37 SIO_GREEN
37 SIO_GREEN_GP000

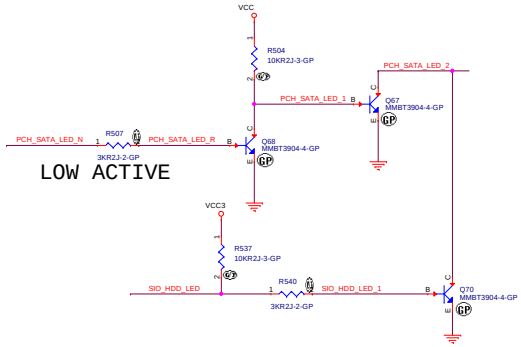
## OSD

20 OSD_MENU
21 OSD_UP
20 OSD_DN
26 OSD_BIST_N
18 PWRCN_DET_N

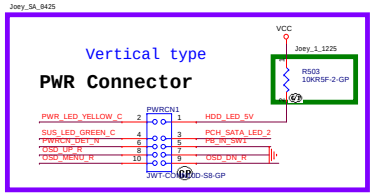


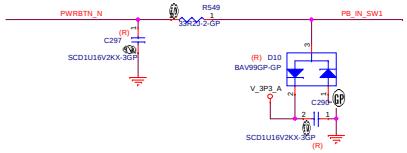

| | Function |
|---|---|
| BTN1 | UP |
| BTN2 | DOWN |
| BTN3 | MENU |

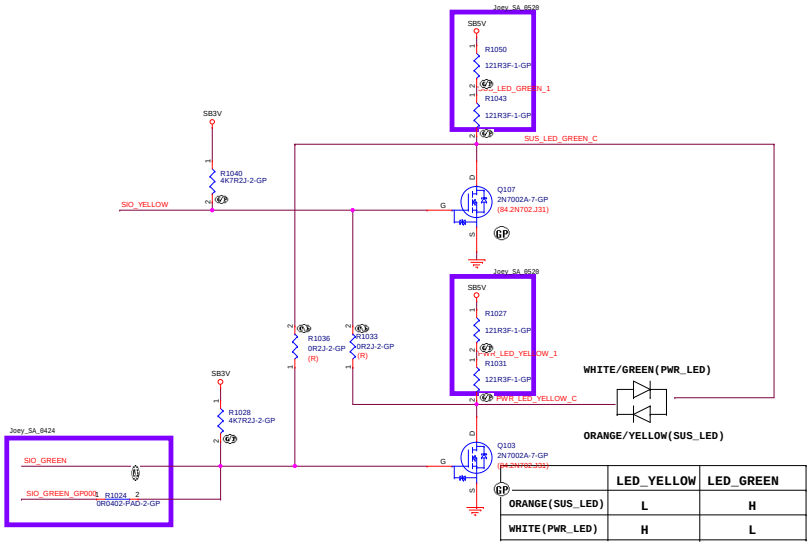
## HDD LED




LOW ACTIVE




| | LED_YELLOW | LED_GREEN |
|---|---|---|
| ORANGE(SUS_LED) | L | H |
| WHITE(PWR_LED) | H | L |

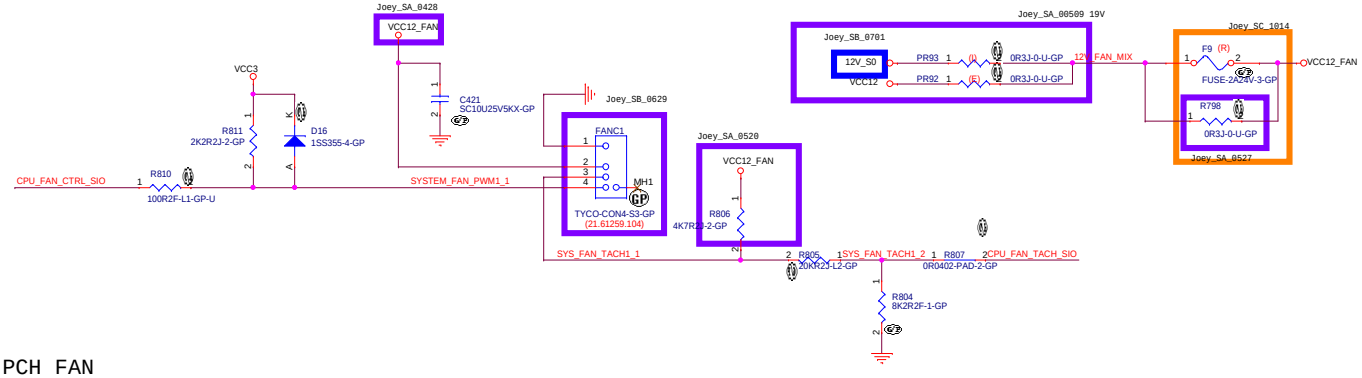
## SIO FAN CONTROL

37 CPU_FAN_CTRL_SIO
37 CPU_FAN_TACH_SIO

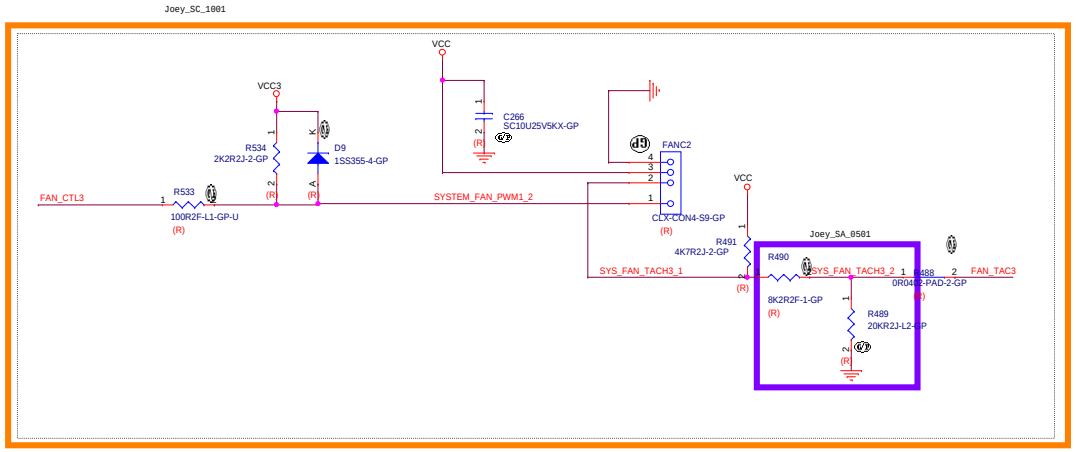
37 FAN_TAC3
37 FAN_CTL3

# 4 PINS FAN CONTROL

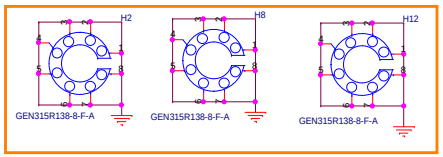
## CPU FAN



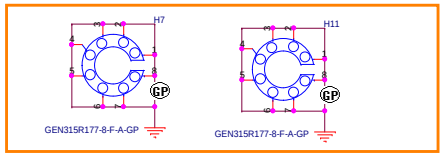

## PCH FAN

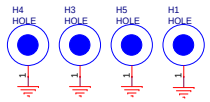



A

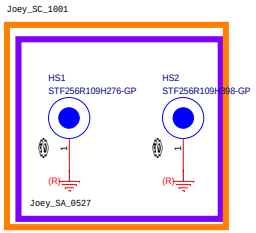



B




**CPU Heatsink screw hole.**

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| wistron | Wistron Incorporated<br>21F, 88, Hsin Tai Wu Rd<br>Hsichih, Taipei | |
| Title | FAN CIRCUITS/HOLE | |
| Size C | Document Number<br>Rosa_Tigris AIO | Rev 1 |
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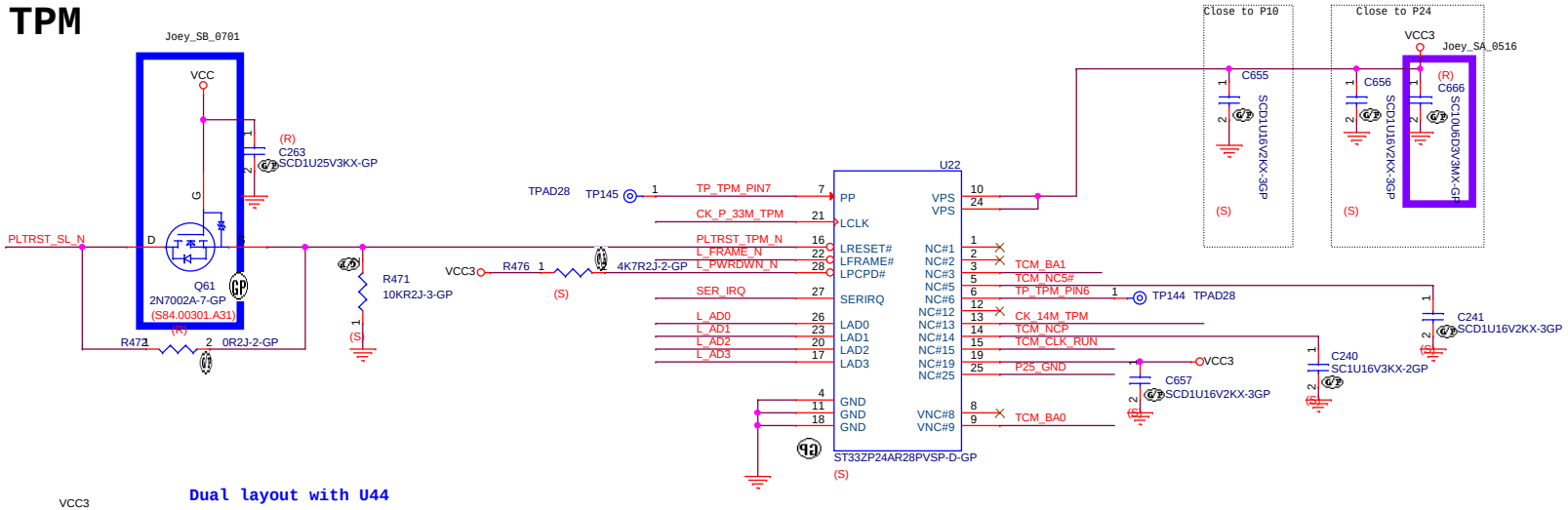
# Serial Port

## LPC

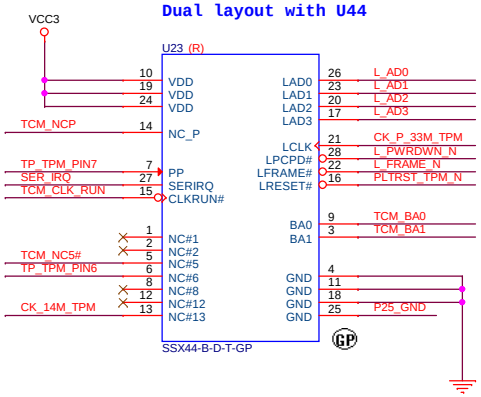
14,18,37 L_AD0
14,18,37 L_AD1
14,18,37 L_AD2
14,18,37 L_AD3
14,18,37 L_FRAME_N

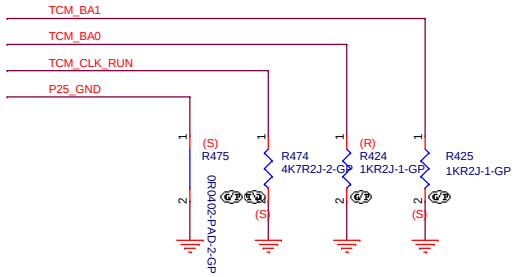
19 CK_P_33M_TPM
20,37 SER_IRQ
14,37,49,52 PLTRST_SL_N
19 CK_14M_TPM

# TPM




## Dual layout with U44

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| | | | |
|---|---|---|---|
| Title | TPM | | |
| Size | Document Number | | Rev |
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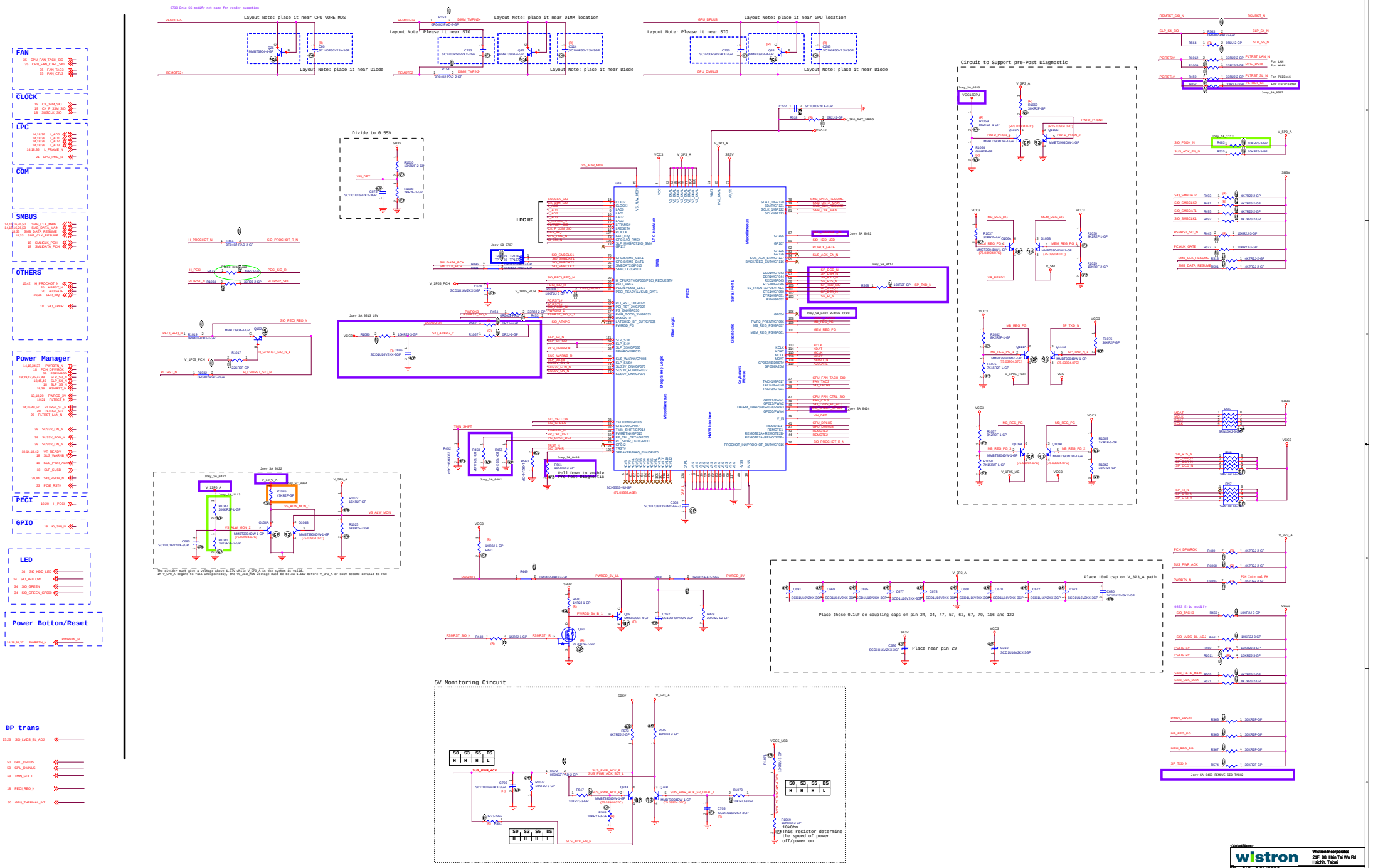
FAN
CLOCK
LPC
COM
SMBUS
OTHERS
Power Manager
PECI
GPIO
LED
Power Botton/Reset
DP trans
Layout Note: place it near CPU VORE MOS
Layout Note: place it near DIMM location
Layout Note: Please it near SIO
Layout Note: place it near GPU location
Layout Note: place it near Diode
Divide to 0.55V
LPC I/F
Circuit to Support pre-Post Diagnostic
Place 10uF cap on V_3P3_A path
Place these 0.1uF de-coupling caps on pin 24, 34, 47, 57, 62, 67, 79, 106 and 122
Place near pin 29
5V Monitoring Circuit
10kOhm
This resistor determine the speed of power off/power on
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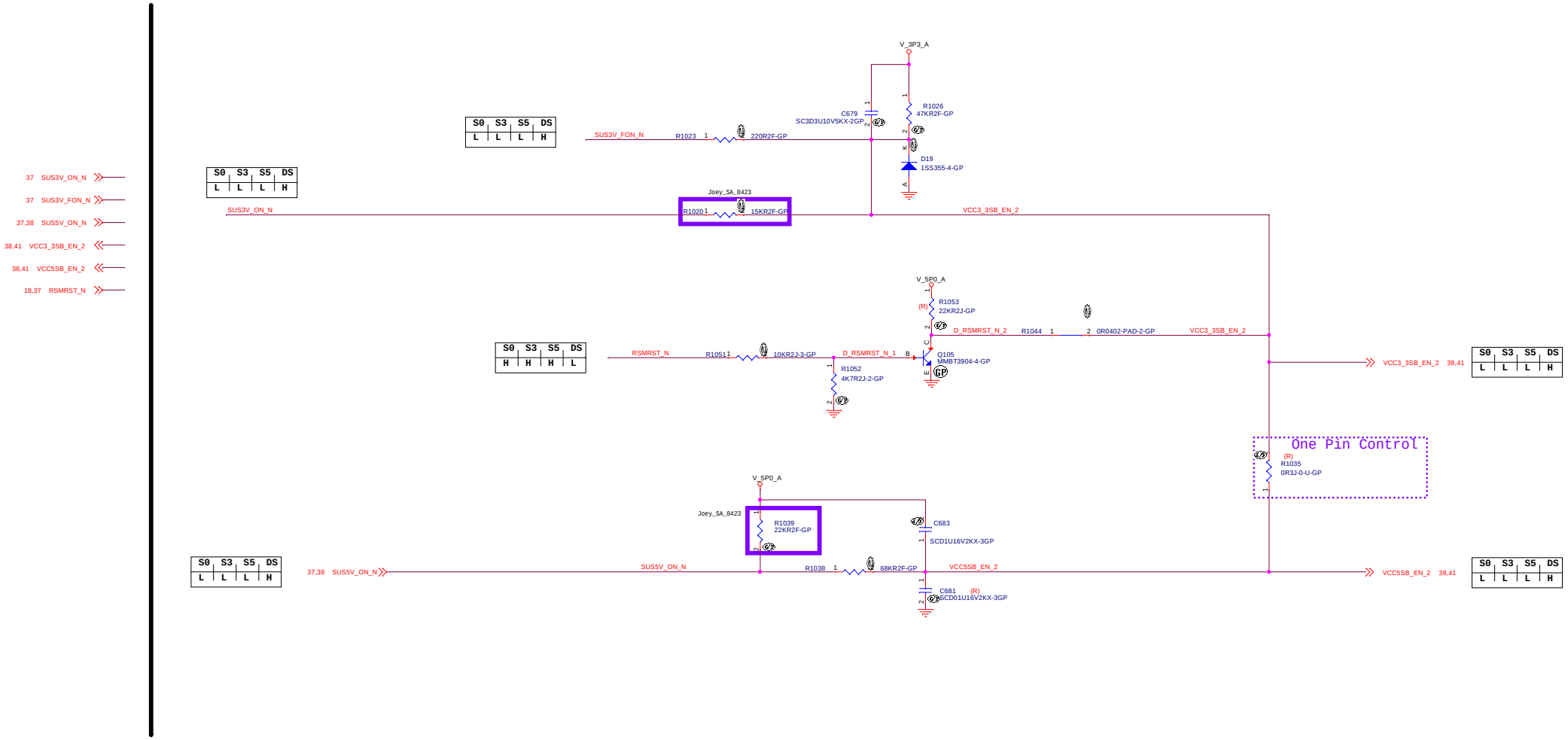
Hsichih, Taipei
SIO_SCH5553
Monday, January 06, 2014

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Title: DSW

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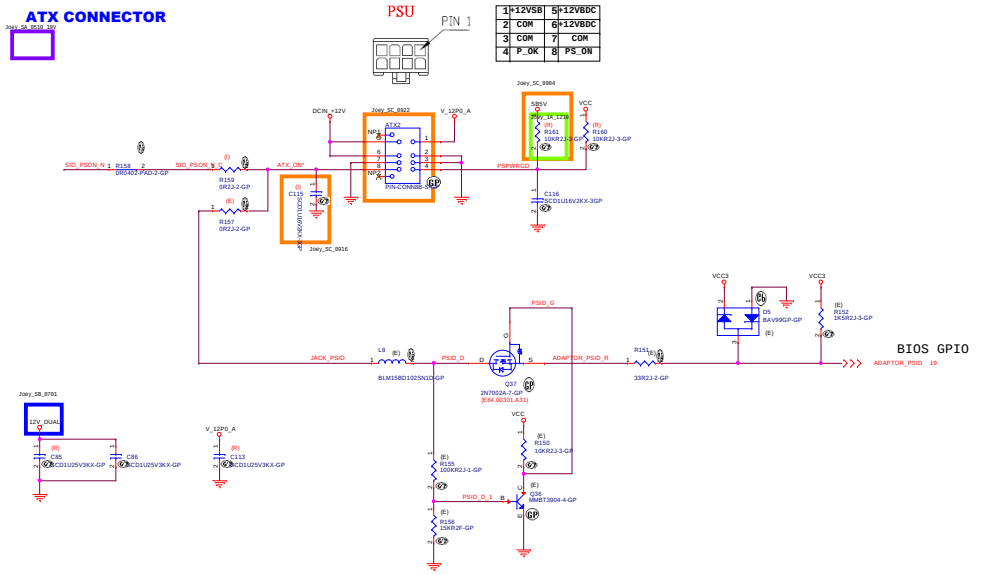
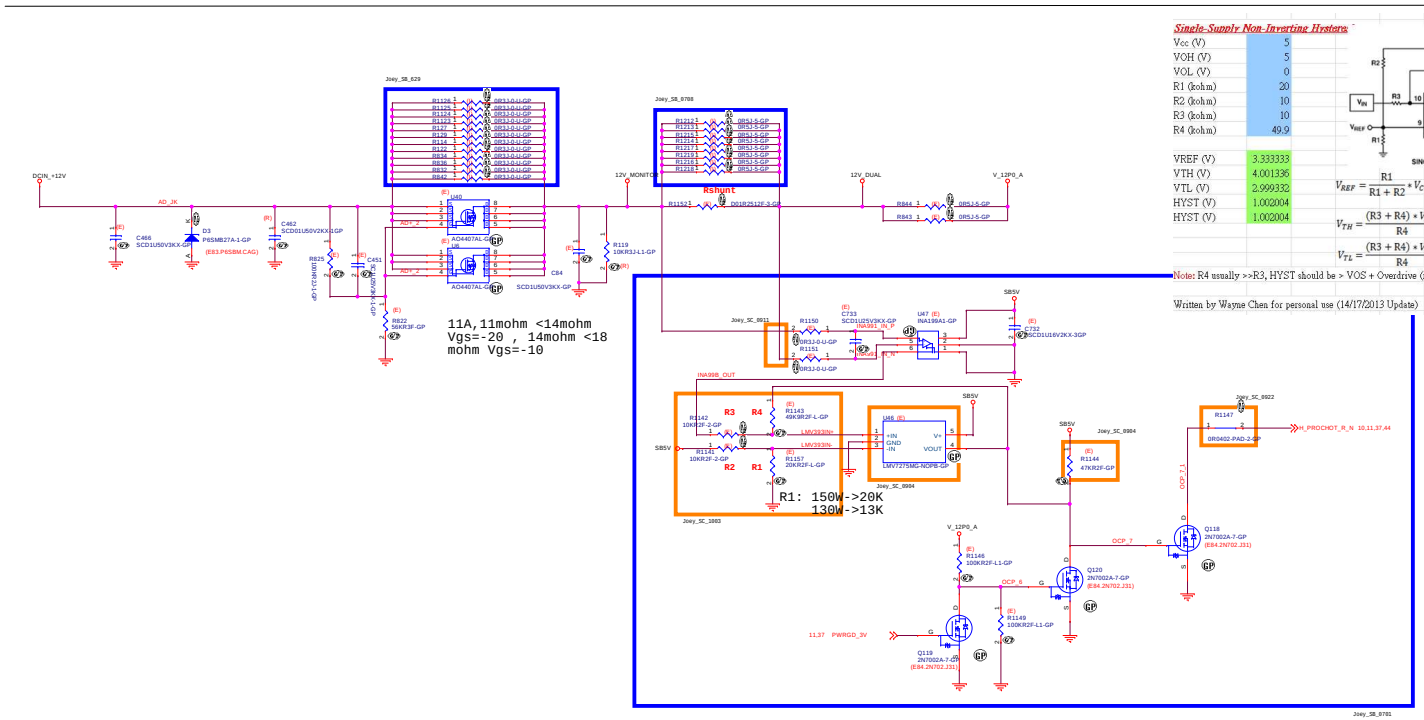
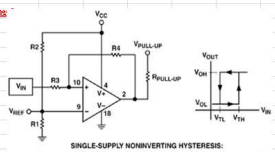



| | | | |
|---|---|---|---|
| 1 | +12VSB | 6 | +12VBDC |
| 2 | COM | 6 | +12VBDC |
| 3 | COM | 7 | COM |
| 4 | P_OK | 8 | PS_ON |




*Single-Supply Non-Inverting Hysteresis*

| | |
|---|---|
| Vcc (V) | 5 |
| VOH (V) | 5 |
| VOL (V) | 0 |
| R1 (kohm) | 20 |
| R2 (kohm) | 10 |
| R3 (kohm) | 10 |
| R4 (kohm) | 49.9 |
| VREF (V) | 3.333333 |
| VTH (V) | 4.001336 |
| VTL (V) | 2.999332 |
| HYST (V) | 1.002004 |
| HYST (V) | 1.002004 |




$$V_{REF} = \frac{R1}{R1 + R2} * V_{CC}$$

$$V_{TH} = \frac{(R3 + R4) * V_{REF}}{R4} - \frac{R3 * V_{OL}}{R4}$$

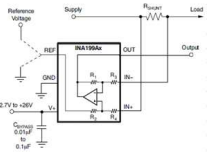
$$V_{TL} = \frac{(R3 + R4) * V_{REF}}{R4} - \frac{R3 * V_{OH}}{R4}$$

$$HYST = V_{TH} - V_{TL}$$

$$HYST = \frac{R3 * (V_{OH} - V_{OL})}{R4}$$

Note: R4 usually >>R3, HYST should be > VOS + Overdrive (refer to op-amp datasheet)

Written by Wayne Chen for personal use (14/17/2013 Update)



| | | | |
|---|---|---|---|
| Rshunt (ohm) | 0.01 | Vcm(V) | 19.5 |
| | A1: 50V/V A2: 100V/V A3: 200V/V | | |
| Ishunt (A) REF | 6.666667 | 3.333333 | 1.666666667 |
| Ishunt (A) TH | 8.002672 | 4.001336 | 2.000668003 |
| Ishunt (A) TL | 5.998664 | 2.999332 | 1.499665999 |
| Ishunt (W) REF | 130 | 65 | 32.5 |
| Ishunt (W) TH | 156.0521 | 78.02605 | 39.01302605 |
| Ishunt (W) TL | 116.9739 | 58.48697 | 29.24348697 |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Title: DC IN

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<Variant Name>

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Title TBD

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|---|---|---|
| Custom | Rosa_Tigris AIO | 1 |

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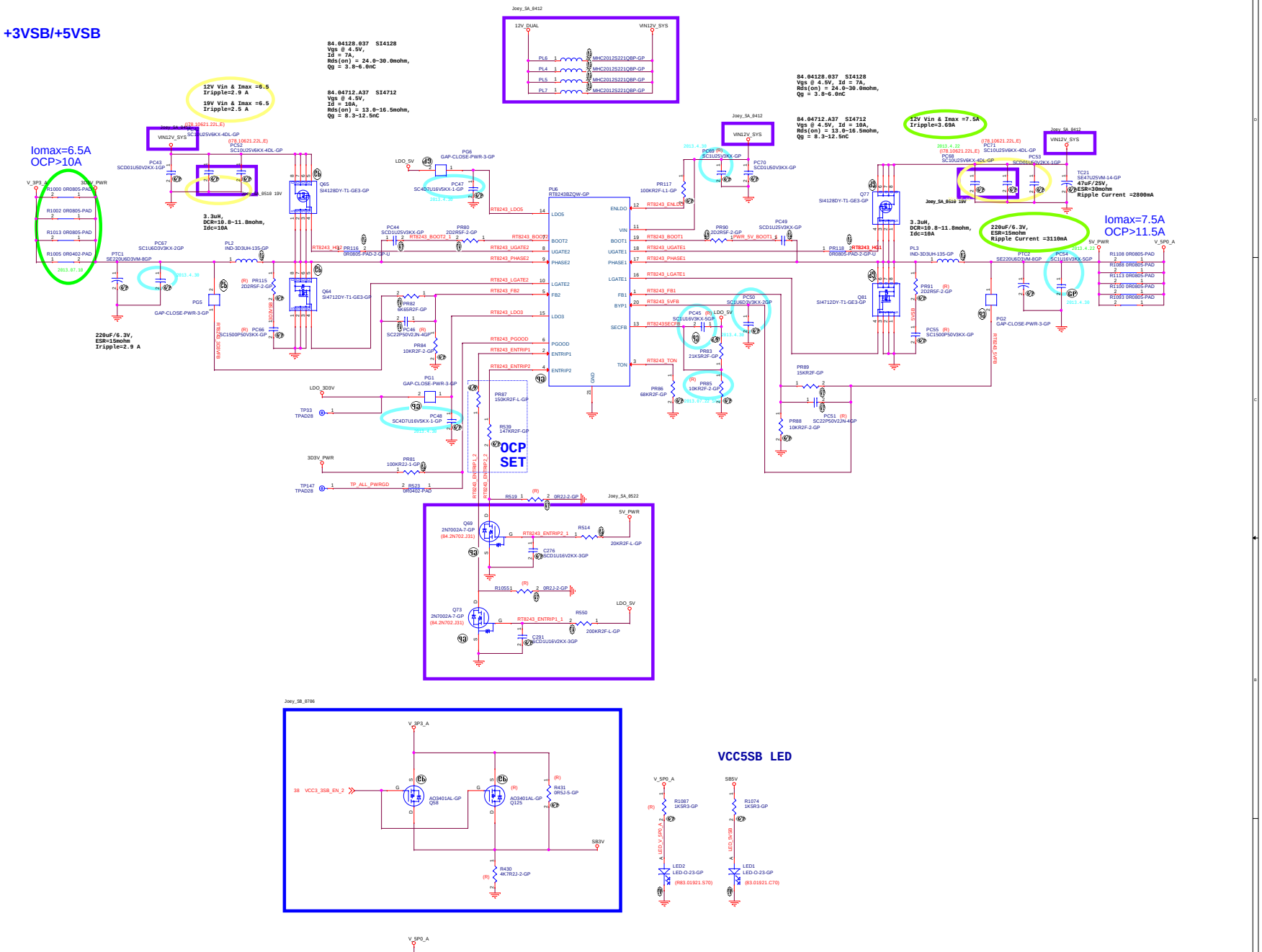
# +3VSB/+5VSB


Iomax=6.5A
OCP>10A
12V Vin & Imax =6.5
Iripple=2.9 A
19V Vin & Imax =6.5
Iripple=2.5 A
84.04128.037 SI4128
Vgs @ 4.5V,
Id = 7A,
Rds(on) = 24.0-30.0mohm,
Qg = 3.8-6.0nC
84.04712.A37 SI4712
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 13.0-16.5mohm,
Qg = 8.3-12.5nC
3.3uH,
DCR=10.8-11.8mohm,
Idc=10A
220uF/6.3V,
ESR=15mohm
Iripple=2.9 A
12V Vin & Imax =7.5A
Iripple=3.69A
220uF/6.3V,
ESR=15mohm
Ripple Current =3110mA
Iomax=7.5A
OCP>11.5A
OCP
SET
VCC5SB LED

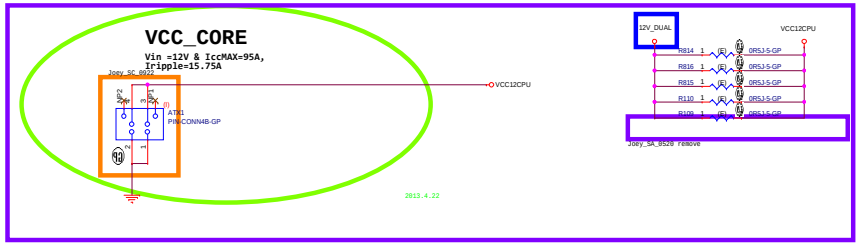
## CPU VCORE POWER

10,42 VCC_SENSE
10,42 VSS_SENSE
10,42 H_VIDSOUT_VR
10,42 H_VIDSCK_VR
10,42 H_VIDALERT_N_VR
42,43 PWM1
42,43 CSN1
42,43 CSP1
42,43 PWM2
42,43 CSN2
42,43 CSP2
42,43 PWM3
42,43 CSN3
42,43 CSP3
10,14,18,37,42 VR_READY

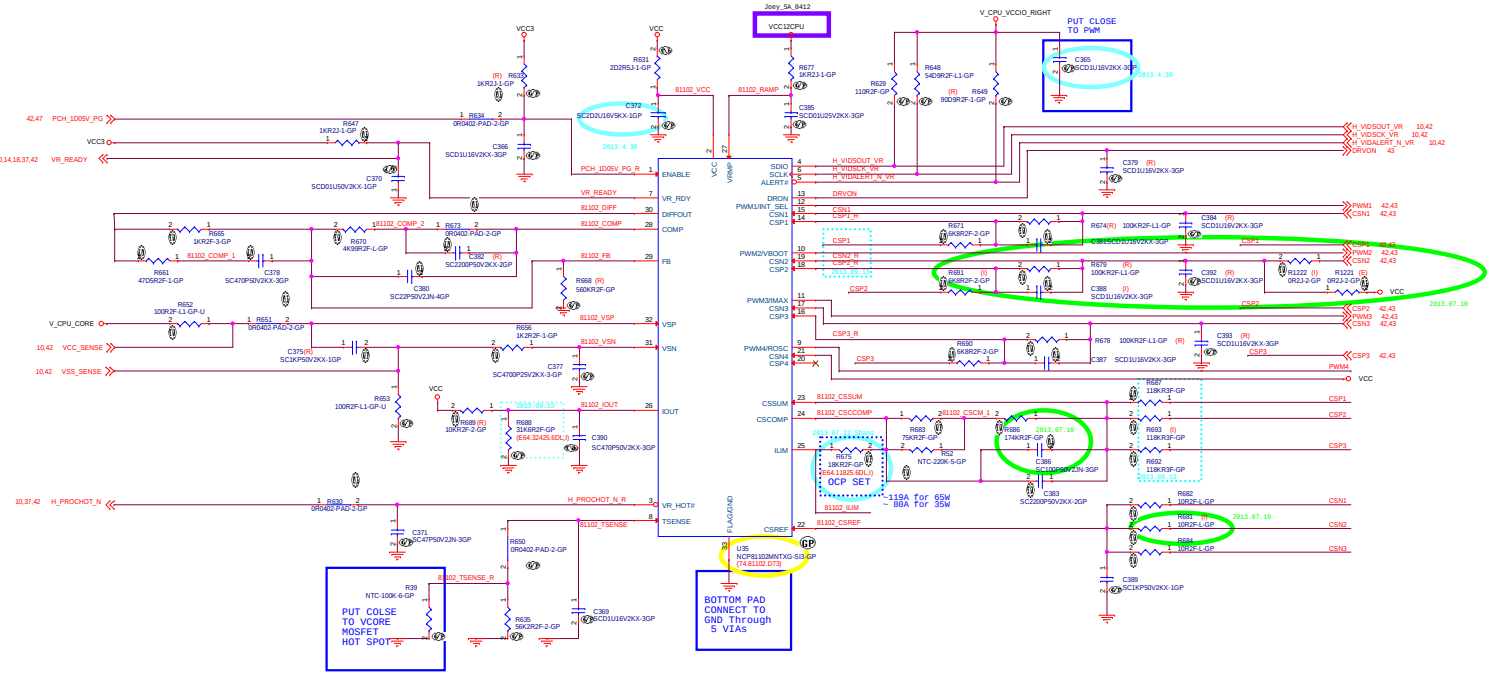
## HOT

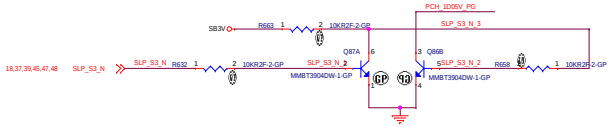
10,37,42 H_PROCHOT_N

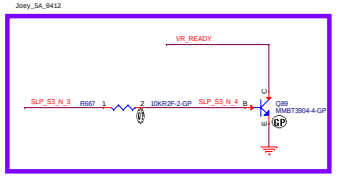
42,47 PCH_1D05V_PG

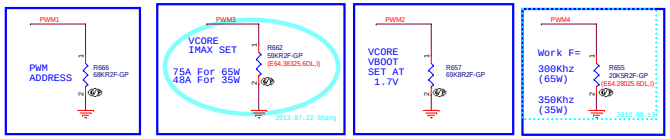



# SharkBay VR12.5 POWER CKT - 3 PHASE





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Title: CPU VRM 12-5 _1
Size: Custom | Document Number: Rosa_Tigris AIO | Rev: 1
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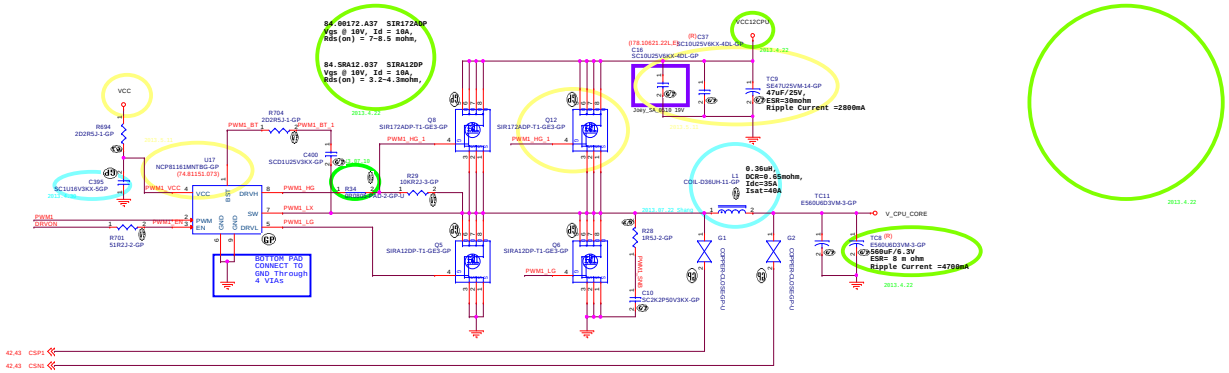
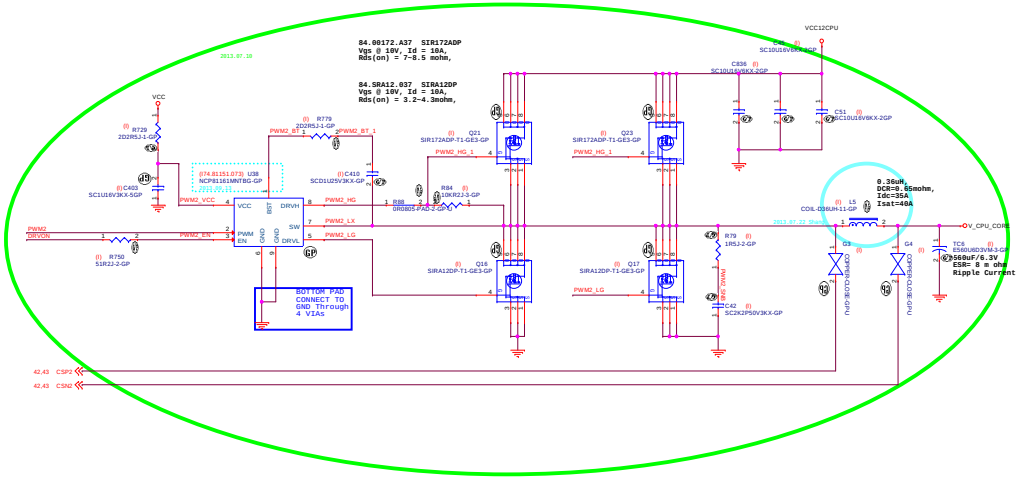
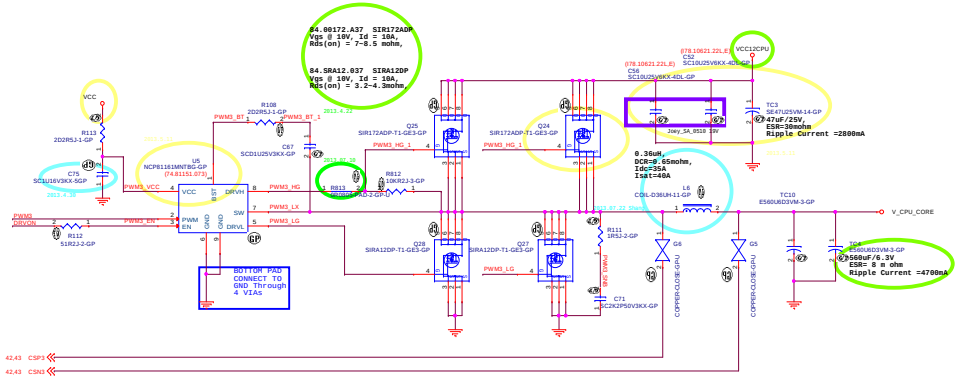
## CPU VCORE POWER

42 DRVON
42 PWM1
42,43 CSP1
42,43 CSN1
42 PWM2
42,43 CSP2
42,43 CSN2
42 PWM3
42,43 CSP3
42,43 CSN3

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| Title | CPU VRM 12-5 _2 |
| Size D | Document Number Rosa_Tigris AIO |
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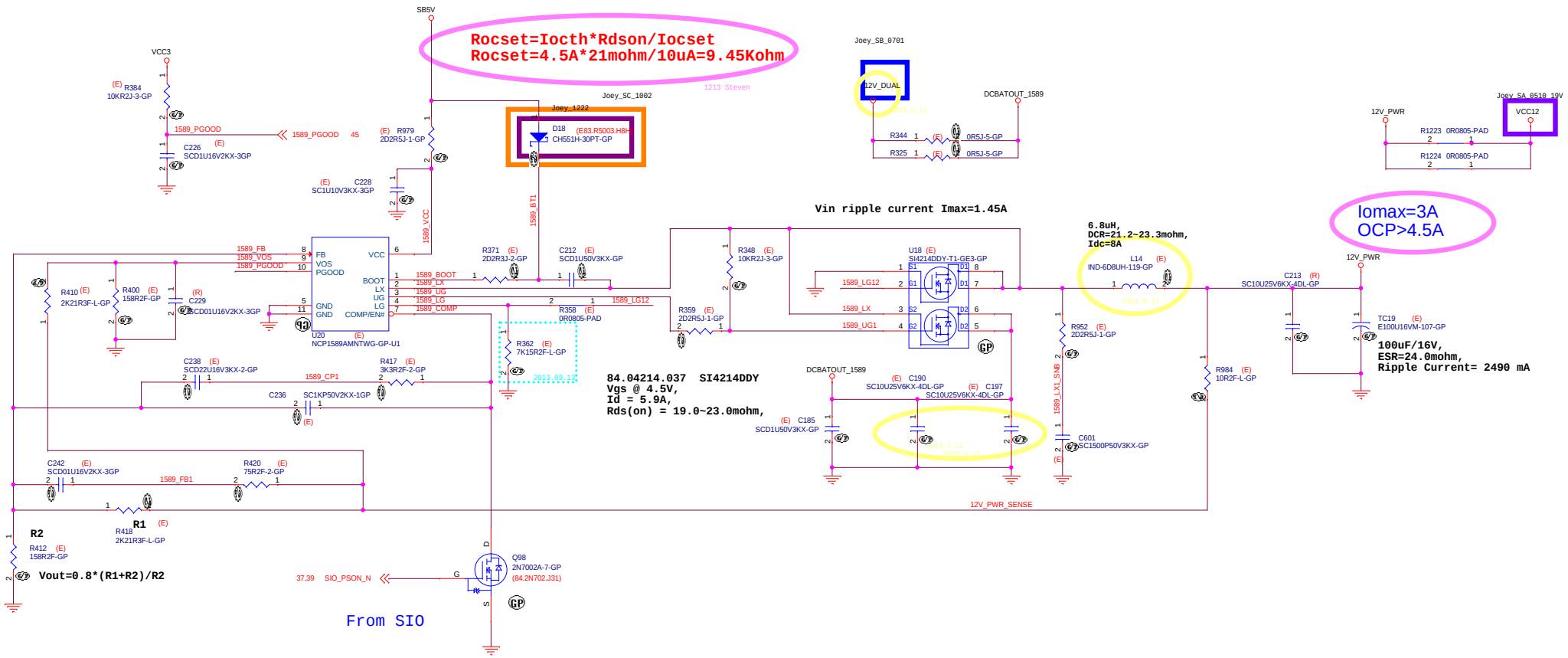
| Date: Monday, January 06, 2014 | Sheet 43 of 58 |

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Title: NCP1589-> +12V

| Size | Document Number | Rev |
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| Custom | Rosa_Tigris AIO | 1 |

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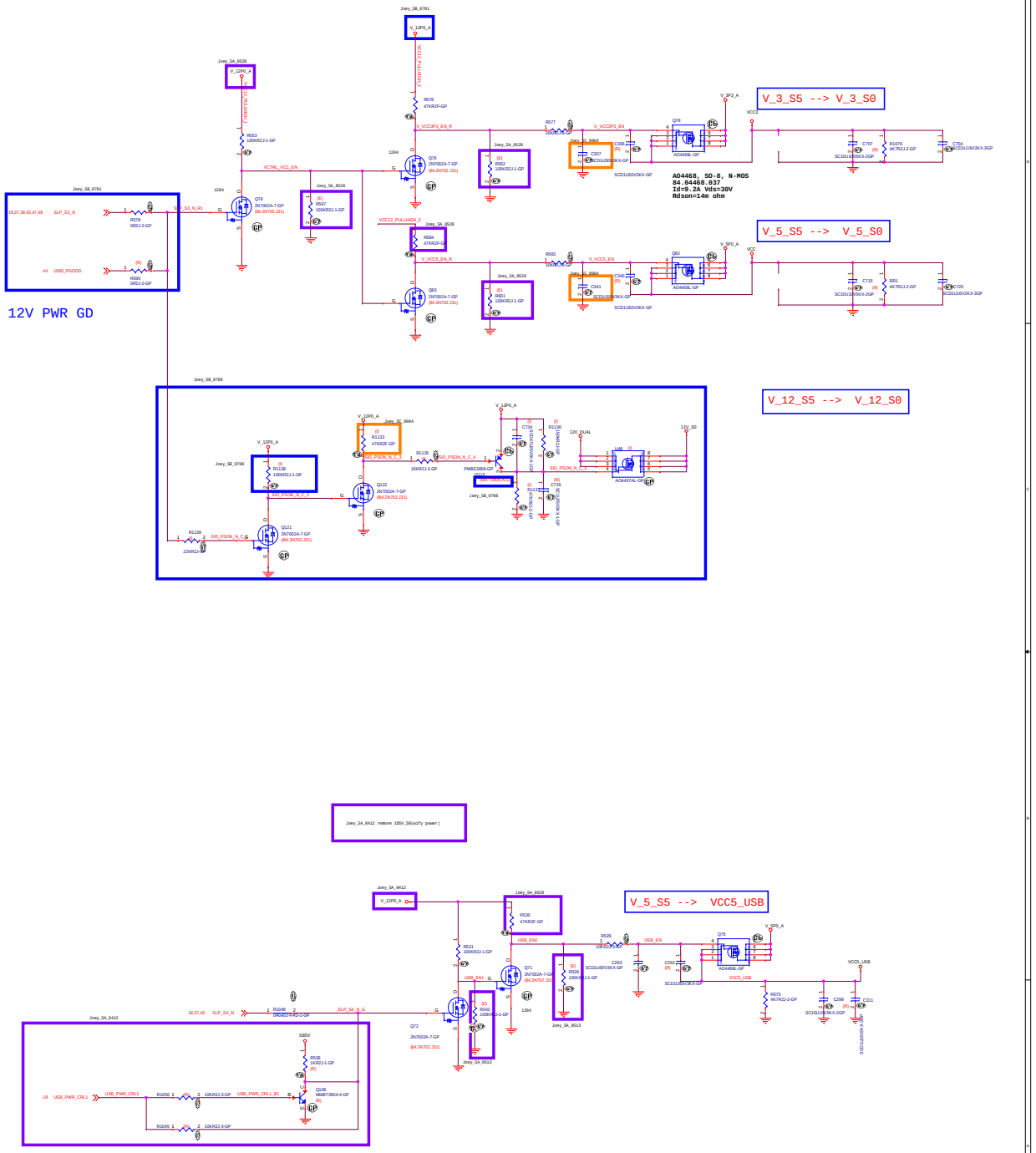
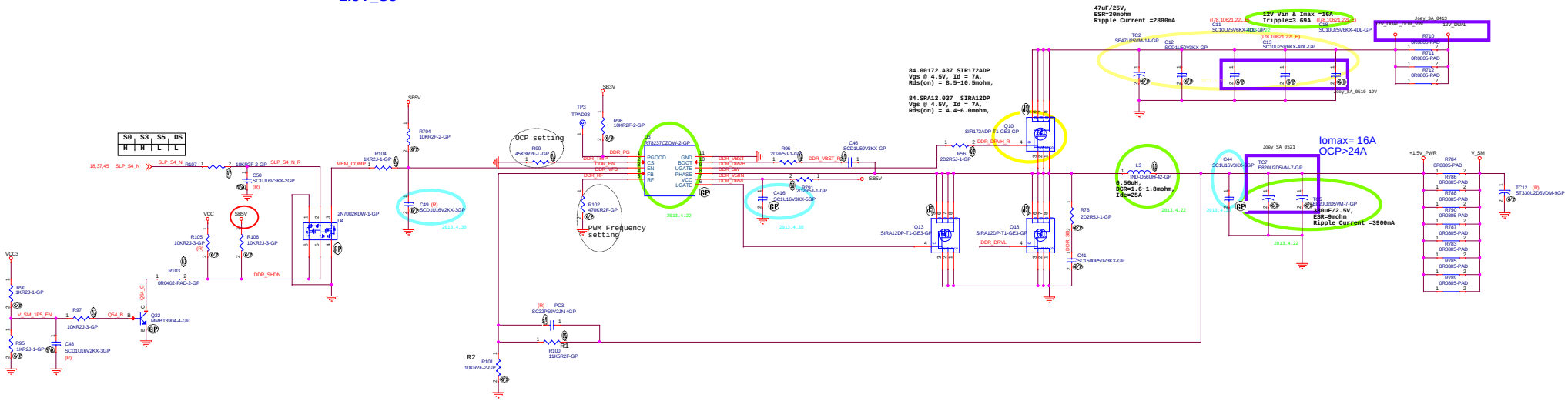
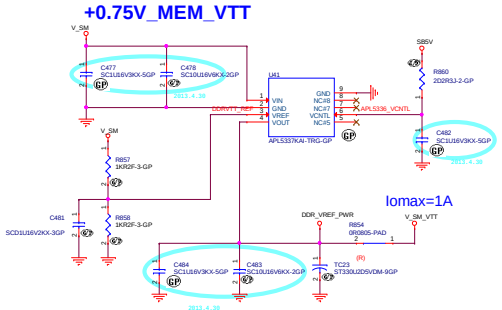

V_3_S5 --> V_3_S0
V_5_S5 --> V_5_S0
V_12_S5 --> V_12_S0
12V PWR GD
AO4468, SO-8, N-MOS
84.04468.037
Id=9.2A Vds=30V
Rdson=14m ohm
Joey_SA_8412 remove 1S5V_S0(wify power)
V_5_S5 --> VCC5_USB

# +1.5V_S3




# +0.75V_MEM_VTT





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Title: MEM_1D5V/MEM_VTT

| Size | Document Number | Rev |
|---|---|---|
| Custom | Rosa_Tigris AIO | 1 |

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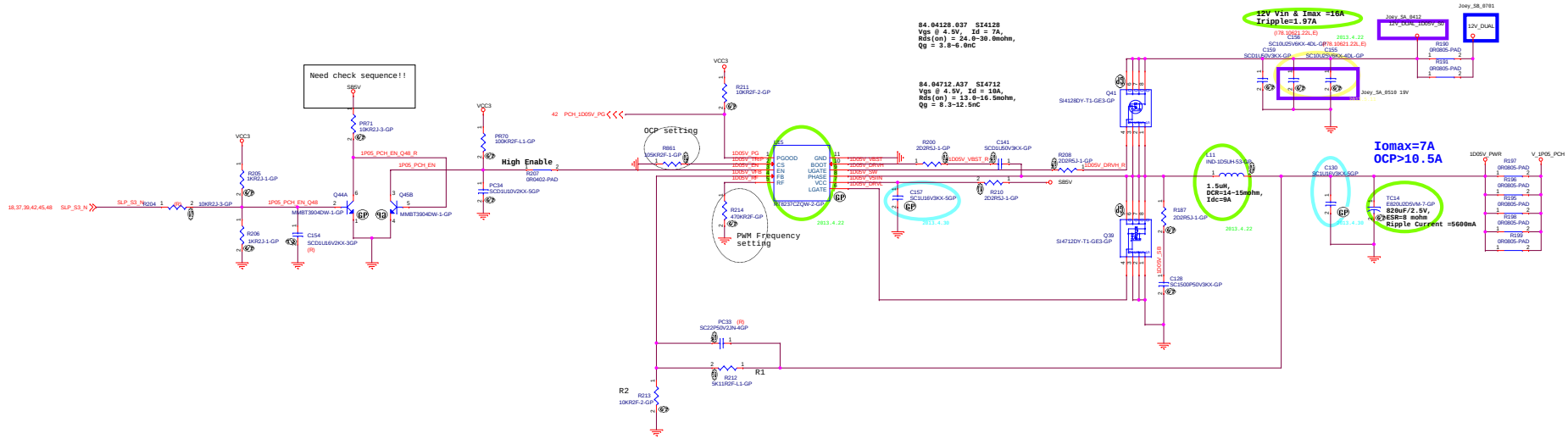
# +1.05V(V_1D05_PCH)_TPS51211DSCR

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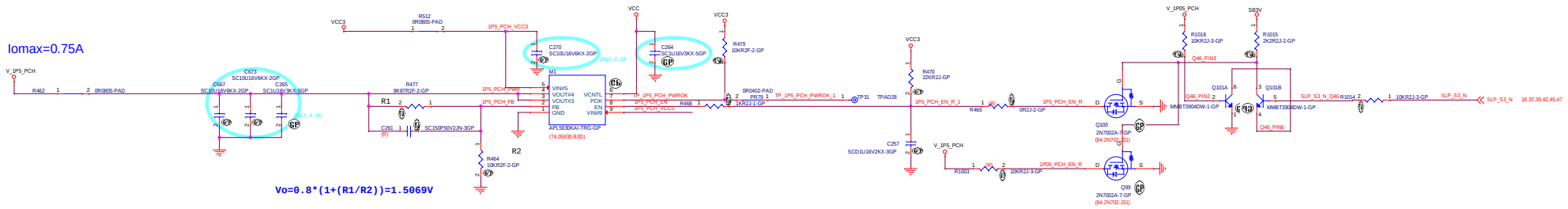
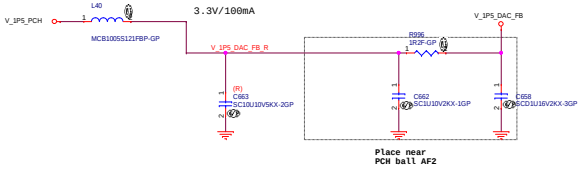
| | | |
|---|---|---|
| Title | PCH_1D05V | |
| Size | Document Number | Rev |
| Custom | Rosa_Tigris AIO | 1 |
| Date: Monday, January 06, 2014 | Sheet 47 of 58 | |

# V_1P5_PCH_Iomax=0.75A




Vo=0.8*(1+(R1/R2))=1.5069V

# V_1P5_DAC_FB_R

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Title: 1D5V PCH POWER

| Size | Document Number | Rev |
|---|---|---|
| | Custom Rosa_Tigris AIO | 1 |

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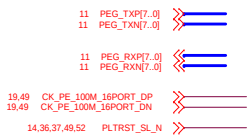
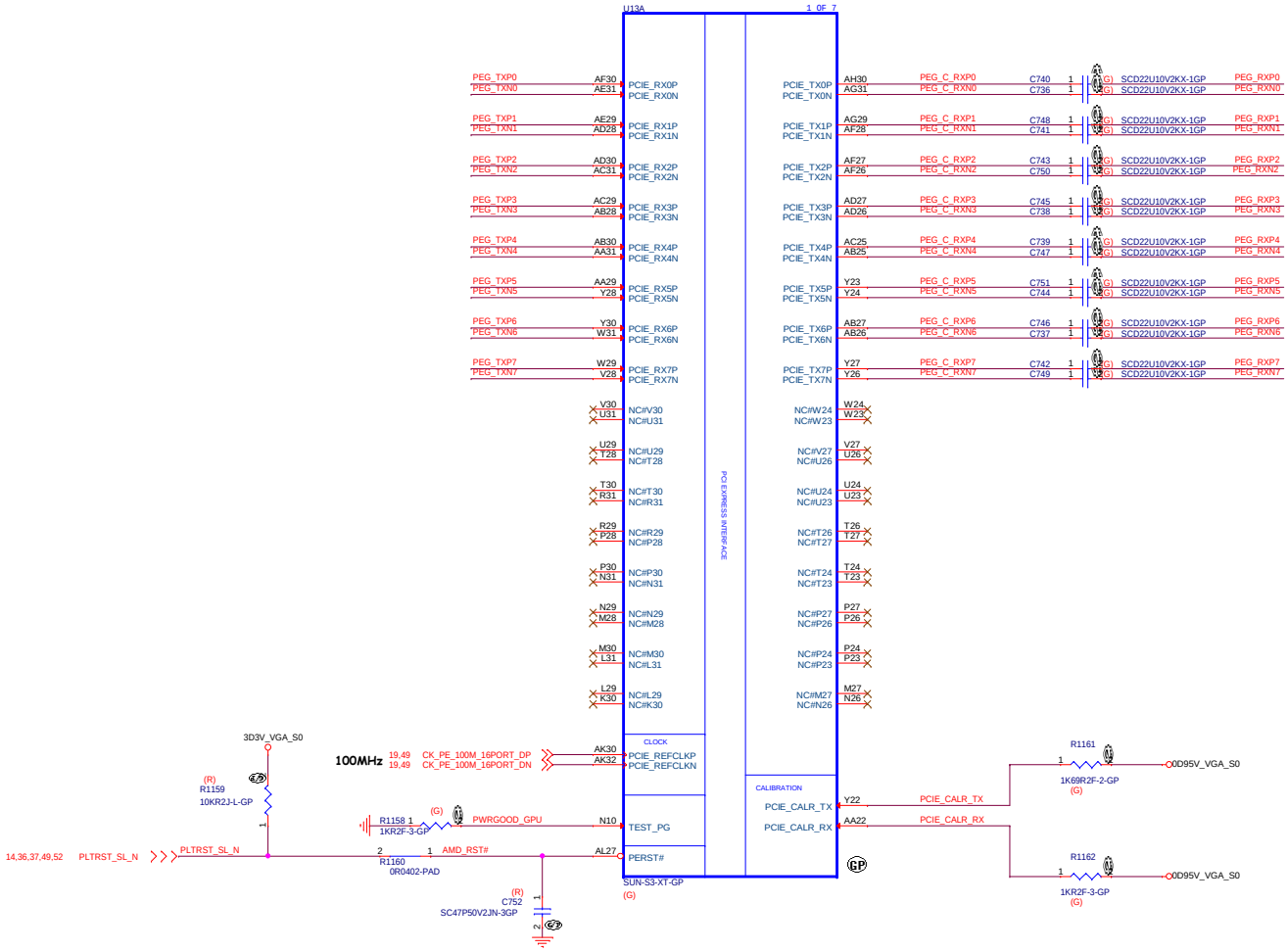
# PCIEX16

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wistron

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Hsichih, Taipei

Title GPU JET PCIE

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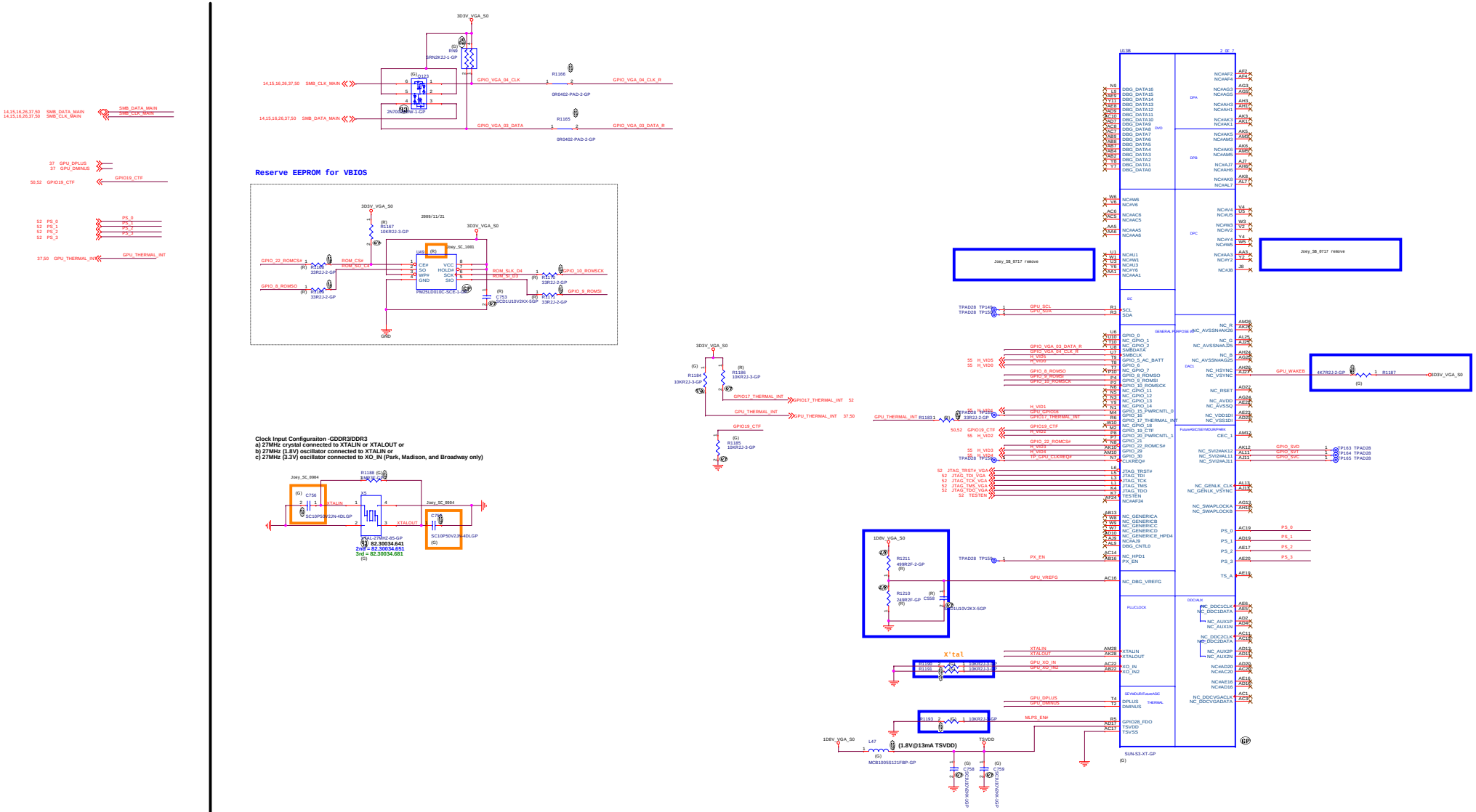
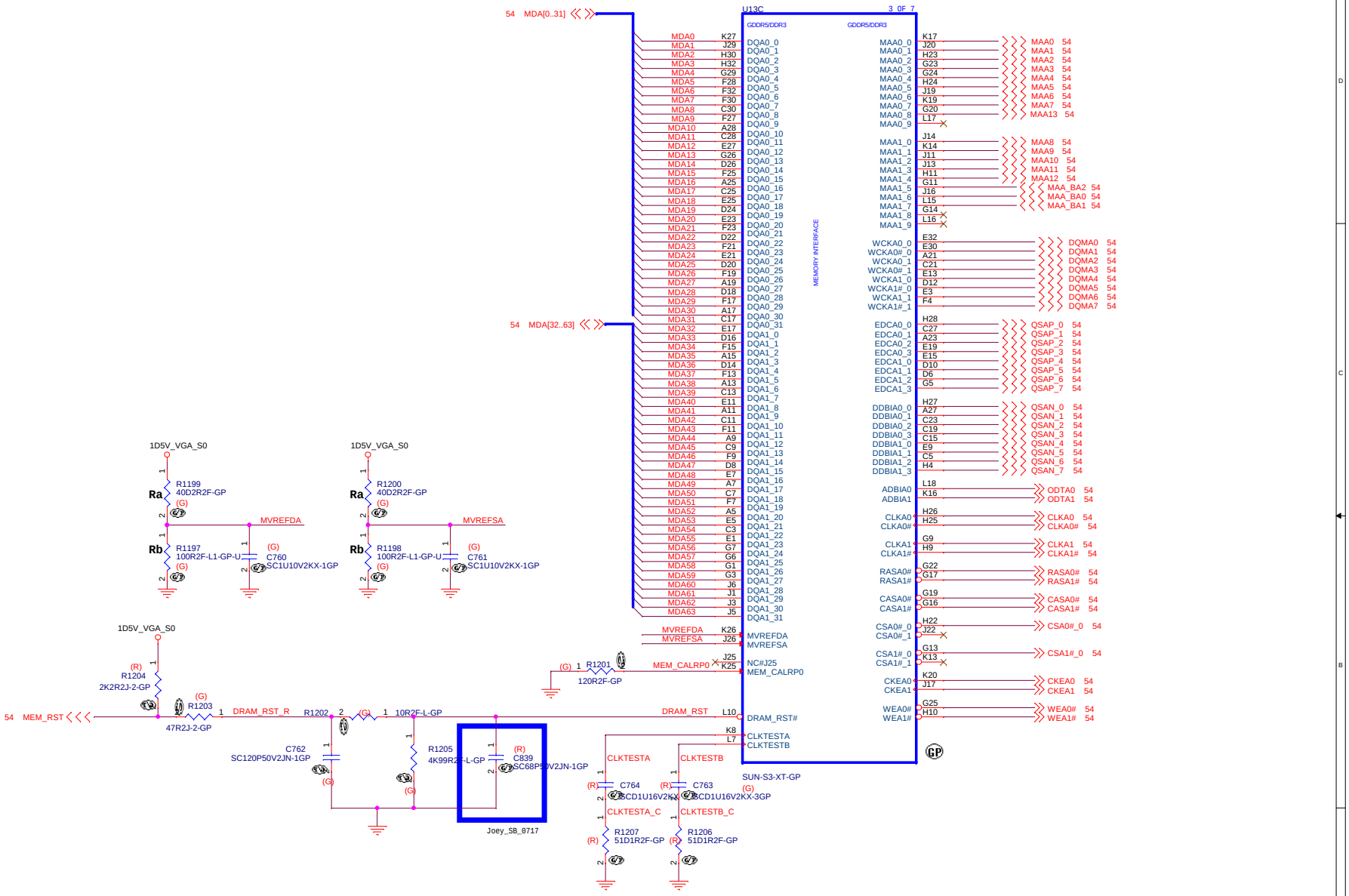

3D3V_VGA_S0
14,15,16,26,37,50 SMB_CLK_MAIN
14,15,16,26,37,50 SMB_DATA_MAIN
GPIO_VGA_04_CLK
GPIO_VGA_04_CLK_R
GPIO_VGA_03_DATA
GPIO_VGA_03_DATA_R
R166
0R0402-PAD-2-GP
R165
0R0402-PAD-2-GP
Reserve EEPROM for VBIOS
2009/11/21
GPIO_22_ROMCS#
ROM_CS#
GPIO_8_ROMSO
ROM_SLK_D4
GPIO_10_ROMSCK
GPIO_9_ROMSI
PM25LD010C-SCE-2-GP
GND
Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)
XTALIN
XTALOUT
82.30034.641
2nd = 82.30034.631
3rd = 82.30034.681
U13B
DBG_DATA16
DBG_DATA15
DBG_DATA14
DBG_DATA13
DBG_DATA12
DBG_DATA11
DBG_DATA10
DBG_DATA9
DBG_DATA8
DBG_DATA7
DBG_DATA6
DBG_DATA5
DBG_DATA4
DBG_DATA3
DBG_DATA2
DBG_DATA1
DBG_DATA0
Joey_SB_0717 remove
GPIO_VGA_03_DATA_R
GPIO_VGA_04_CLK_R
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_15_PWRCNTL_0
GPIO_17_THERMAL_INT
GPIO_19_CTF
GPIO_22_ROMCS#
GPIO_20_PWRCNTL_1
GPIO_21
GPIO_22_ROMCS#
GPIO_29
GPIO_30
CLKREQ#
JTAG_TRST#
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN
NC_DBG_VREFG
PLL/CLOCK
X'tal
XTALIN
XTALOUT
XO_IN
XO_IN2
SE/VIDEO/Future/AGE
DPLUS
DMINUS
THERMAL
GPIO28_FDO
TSVDD
TSVSS
SUN-S3-XT-GP
1DBV_VGA_S0
(1.8V@13mA TSVDD)
MCB1005S121FBP-GP
GPU_WAKEB
4K7B22-2-GP
R1187
3D3V_VGA_S0
GPIO_SVD
GPIO_SVT
GPIO_SVC
P163 TPAD28
P164 TPAD28
P165 TPAD28
PS_0
PS_1
PS_2
PS_3
TS_A
NC_DDC1CLK
NC_DDC1DATA
NC_AUX1P
NC_AUX1N
NC_DDC2CLK
NC_DDC2DATA
NC_AUX2P
NC_AUX2N
NC_DDCVGACLK
NC_DDCVGADATA
NC_R
NC_G
NC_B
NC_HSYNC
NC_VSYNC
NC_RSET
NC_AVDD
NC_AVSSQ
NC_VDD10D
NC_VSS1D
NC_SV2#AK14
NC_SV2#AL11
NC_SV2#AJ11
NC_GENLK_CLK
NC_GENLK_VSYNC
NC_SWAPLOCKA
NC_SWAPLOCKB
NC_AVSSNHAK26
NC_AVSSNHAJ25
NC_AVSSNHAG25
NC_AVSSNHAF25
CEC_1
NC_GPIO_1
NC_GPIO_2
SMBDATA
SMBCLK
GPIO_5
NC_GPIO_7
GPIO_8
GPIO_9
GPIO_10
NC_GPIO_11
NC_GPIO_12
NC_GPIO_13
NC_GPIO_14
GPIO_15
GPIO_17
GPIO_19
GPIO_20
GPIO_21
GPIO_22
GPIO_29
GPIO_30
JTAG_TRST#
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN
NC_HPD1
PX_EN
NC_DBG_VREFG
XTALIN
XTALOUT
XO_IN
XO_IN2
GPIO28_FDO
TSVDD
TSVSS
SUN-S3-XT-GP
1DBV_VGA_S0
(1.8V@13mA TSVDD)
MCB1005S121FBP-GP
TSVDD
GPU_WAKEB
4K7B22-2-GP
R1187
3D3V_VGA_S0
GPIO_SVD
GPIO_SVT
GPIO_SVC
P163 TPAD28
P164 TPAD28
P165 TPAD28
PS_0
PS_1
PS_2
PS_3
TS_A
NC_DDC1CLK
NC_DDC1DATA
NC_AUX1P
NC_AUX1N
NC_DDC2CLK
NC_DDC2DATA
NC_AUX2P
NC_AUX2N
NC_DDCVGACLK
NC_DDCVGADATA
NC_R
NC_G
NC_B
NC_HSYNC
NC_VSYNC
NC_RSET
NC_AVDD
NC_AVSSQ
NC_VDD10D
NC_VSS1D
NC_SV2#AK14
NC_SV2#AL11
NC_SV2#AJ11
NC_GENLK_CLK
NC_GENLK_VSYNC
NC_SWAPLOCKA
NC_SWAPLOCKB
NC_AVSSNHAK26
NC_AVSSNHAJ25
NC_AVSSNHAG25
CEC_1
NC_GPIO_1
NC_GPIO_2
SMBDATA
SMBCLK
GPIO_5
NC_GPIO_7
GPIO_8
GPIO_9
GPIO_10
NC_GPIO_11
NC_GPIO_12
NC_GPIO_13
NC_GPIO_14
GPIO_15
GPIO_17
GPIO_19
GPIO_20
GPIO_21
GPIO_22
GPIO_29
GPIO_30
JTAG_TRST#
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN
NC_HPD1
PX_EN
NC_DBG_VREFG
XTALIN
XTALOUT
XO_IN
XO_IN2
GPIO28_FDO
TSVDD
TSVSS
SUN-S3-XT-GP
1DBV_VGA_S0
(1.8V@13mA TSVDD)
MCB1005S121FBP-GP
TSVDD




<Variant Name>

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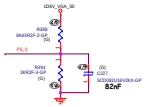
Title GPU_JET MEMORY

s AIO

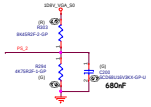
Rev 1

2014 Sheet 51 of 58

**Aperture Size = 256MB**
**01001**




**00000**




| | | | |
|---|---|---|---|
| **PS_0[1]**<br>**PS_0[2]**<br>**PS_0[3]** | ROM_CONFIG[0]<br>ROM_CONFIG[1]<br>ROM_CONFIG[2] | If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type.<br>If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 48). | Design dependent, see the description. |
| **PS_0[4]** | N/A | Reserved for internal use only.<br>Must be 1 at reset. | 1 |
| **PS_0[5]** | AUD_PORT_CONN_ PINSTRAP[0] | The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs. | Design dependent, see the description. |

| | | | |
|---|---|---|---|
| **PS_2[1]** | N/A | Reserved. | N/A |
| **PS_2[2]** | N/A | Reserved. | N/A |
| **PS_2[3]** | STRAP_BIOS_ROM_EN | To enable the external BIOS ROM device.<br>0 = Disable the external BIOS ROM device.<br>1 = Enable the external BIOS ROM device. | Design dependent, see the description. |
| **PS_2[4]** | STRAP_BIF_VGA_DIS | VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space).<br>0 = VGA controller capacity enabled.<br>1 = The device will not be recognized as the system's VGA controller. | 0 |
| **PS_2[5]** | N/A | Reserved | N/A |

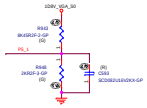
Resistor Divider Lookup Table for Bits [3:1]

| R_pu (Ω) | R_pd (Ω) | Bits [3:1] |
|---|---|---|
| NC | 4750 | 000 |
| 8450 | 2000 | 001 |
| 4530 | 2000 | 010 |
| 6980 | 4990 | 011 |
| 4530 | 4990 | 100 |
| 3240 | 5620 | 101 |
| 3400 | 10000 | 110 |
| 4750 | NC | 111 |
| **Note**: 0402 1% resistors are required. | | |

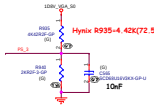
Capacitor Lookup Table for Bits [5:4]

| Capacitor Value (nF) | Bits [5:4] |
|---|---|
| 680 | 00 |
| 82 | 01 |
| 10 | 10 |
| NC | 11 |

**PS_1[1]=1 => PCIe GEN3 is supported**
**11001**




**PS_3[3-1] => MEM_ID setting, need decide for AMD**
**00000**

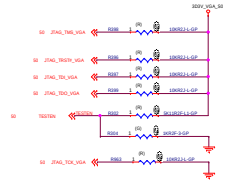



| | | | |
|---|---|---|---|
| **PS_1[1]** | STRAP_BIF_ GEN3_EN_A | PCIe GEN3 capability.<br>1 = PCIe GEN3 is supported.<br>0 = PCIe GEN3 is not supported. | Design dependent, see the description. |
| **PS_1[2]** | STRAP_BIF_CLK_PM_EN | Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB).<br>0 = The CLKREQB power management capability is disabled<br>1 = The CLKREQB power management capability is enabled | 0 |
| **PS_1[3]** | N/A | Reserved for internal use only.<br>Must be 0 at reset. | 0 |
| **PS_1[4]** | STRAP_TX_CFG_DRV_FULL_SWING | Control the transmitter full-/half-swing mode<br>0 = The transmitter half-swing is enabled<br>1 = The transmitter full-swing is enabled | 1 |
| **PS_1[5]** | STRAP_TX_DEEMPH_EN | PCI EXPRESS® transmitter, de-emphasis enable.<br>0 = Tx deemphasis disabled.<br>1 = Tx deemphasis enabled. | Design dependent, see the description. |

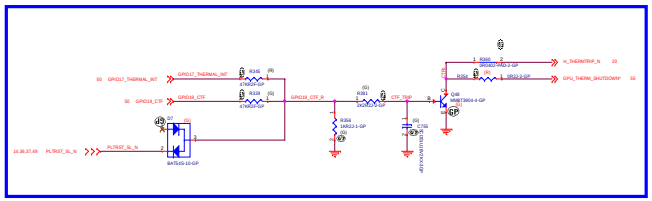
| | | | |
|---|---|---|---|
| **PS_3[1]**<br>**PS_3[2]**<br>**PS_3[3]** | BOARD_CONFIG[0]<br>BOARD_CONFIG[1]<br>BOARD_CONFIG[2] | Board configuration related strapping, such as for memory ID | Design dependent, see the description. |
| **PS_3[4]**<br>**PS_3[5]** | AUD_PORT_CONN_ PINSTRAP[1]<br>AUD_PORT_CONN_ PINSTRAP[2] | Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP/ HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. This pin strap is encoded as an active low binary as follows to ensure zero enables all endpoints.<br>111 = No usable endpoints.<br>110 = One usable endpoint.<br>101 = Two usable endpoints.<br>100 = Three usable endpoints.<br>011 = Four usable endpoints.<br>010 = Five usable endpoints.<br>001 = Six usable endpoints.<br>000 = All endpoints are usable. | Design dependent, see the description. |

**JTAG SIGNAL OPTION**

| Signal | Normal mode | Debug mode | pilot run mode |
|---|---|---|---|
| TESTEN | "0"(PD) | "1"(PU) | "0"(PD) |
| JTAG_TRST# | "1"(PU) | "1"(PU) | NC |
| JTAG_TCK | "0"(PD) | "1"(PU) | NC |
| JTAG_TMS | "1"(PU) | "1"(PU) | NC |



# THERMAL PROTECTION





<Variant Name>
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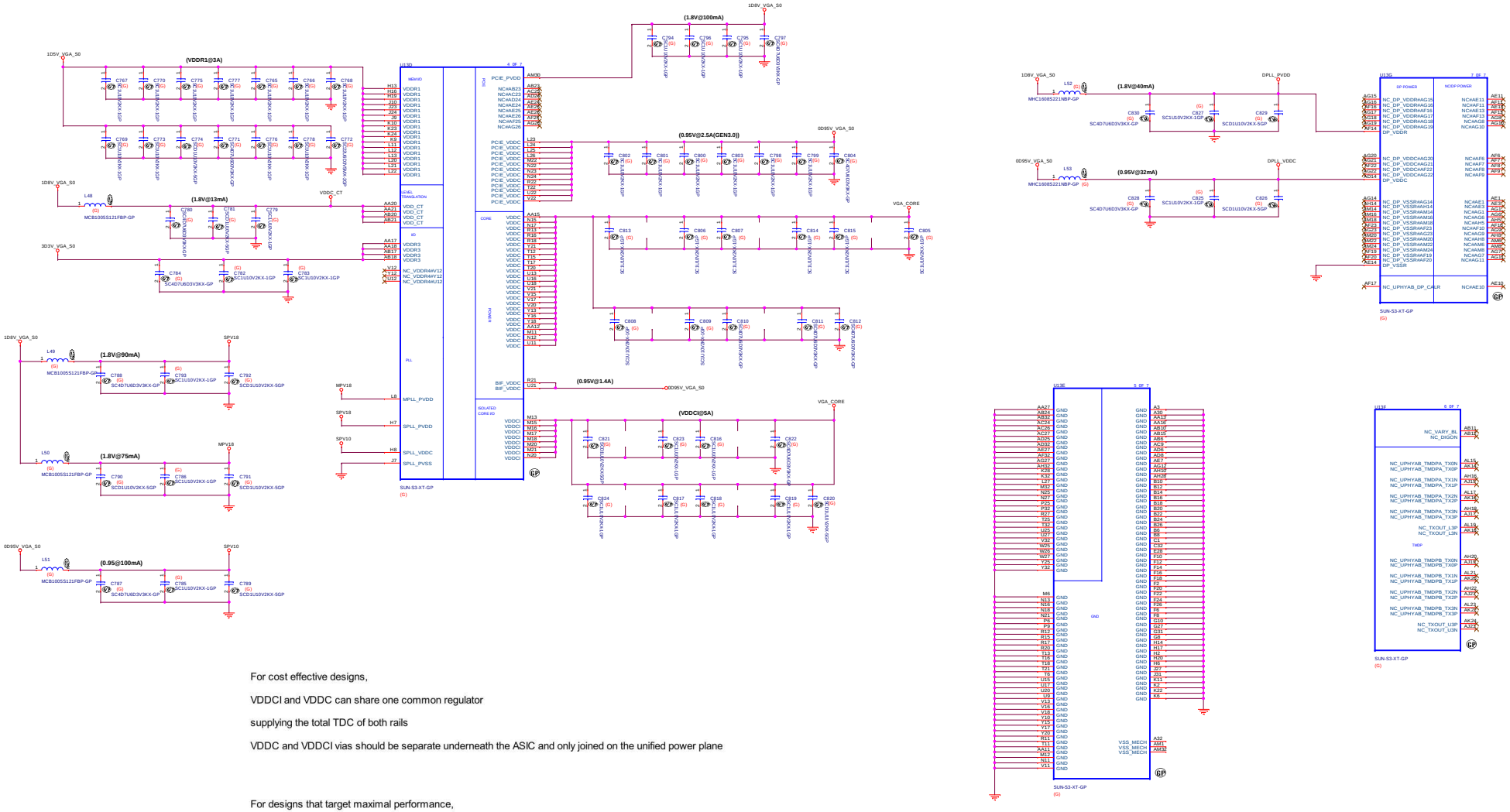
Title: GPU_JET IO

Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Friday, August 19, 2011 | Sheet 34 of 38




For cost effective designs,

VDDCI and VDDC can share one common regulator

supplying the total TDC of both rails

VDDC and VDDCI vias should be separate underneath the ASIC and only joined on the unified power plane

For designs that target maximal performance,

a dedicated regulator for VDDCI with two selectable output levels is required.

VDDCI FB is available on Topaz.

<Variant Name>

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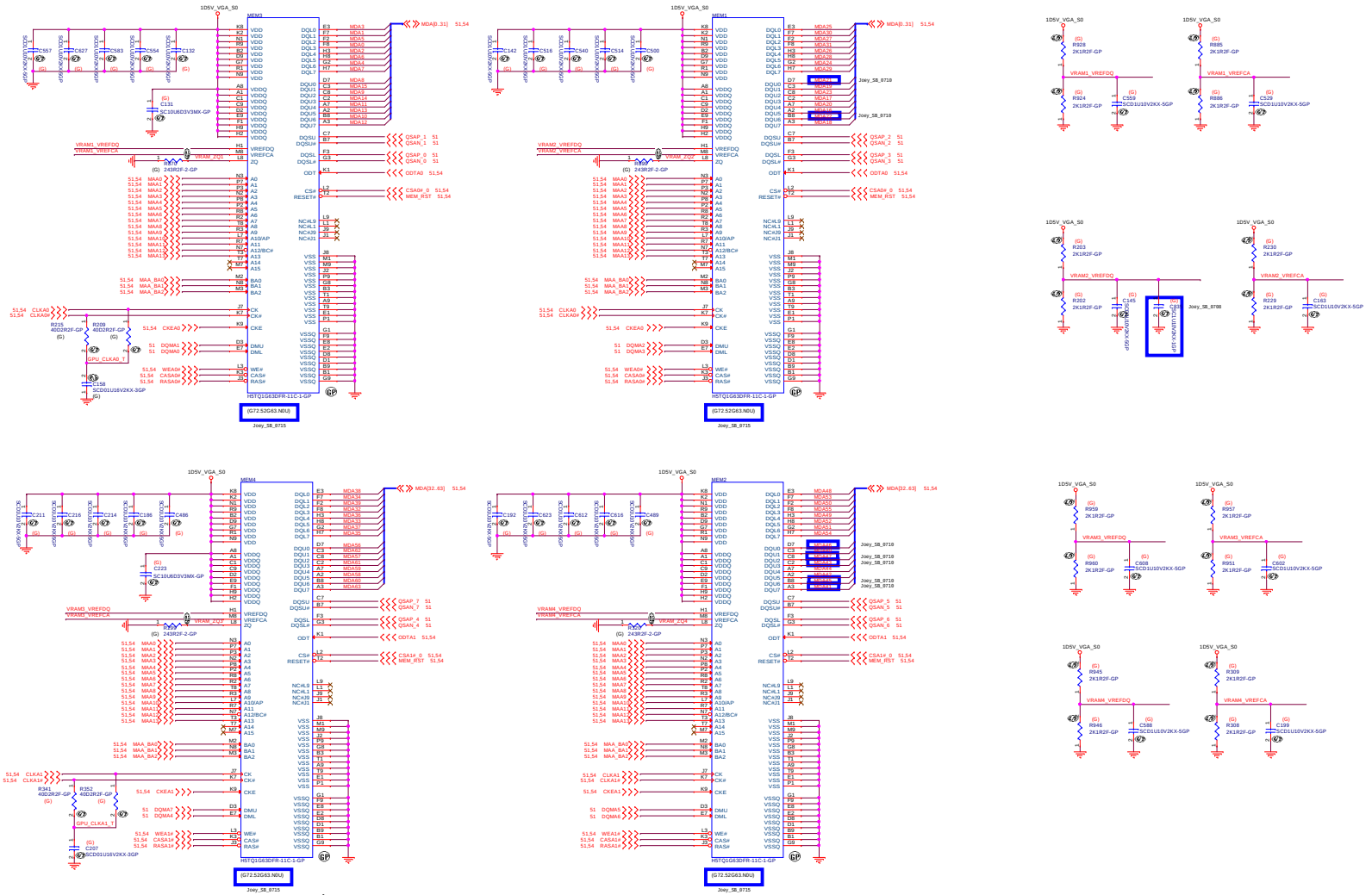
Hsichih, Taipei

Title: GPU_JET POWER

Size: D | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 53 of 58





<Variant Name>
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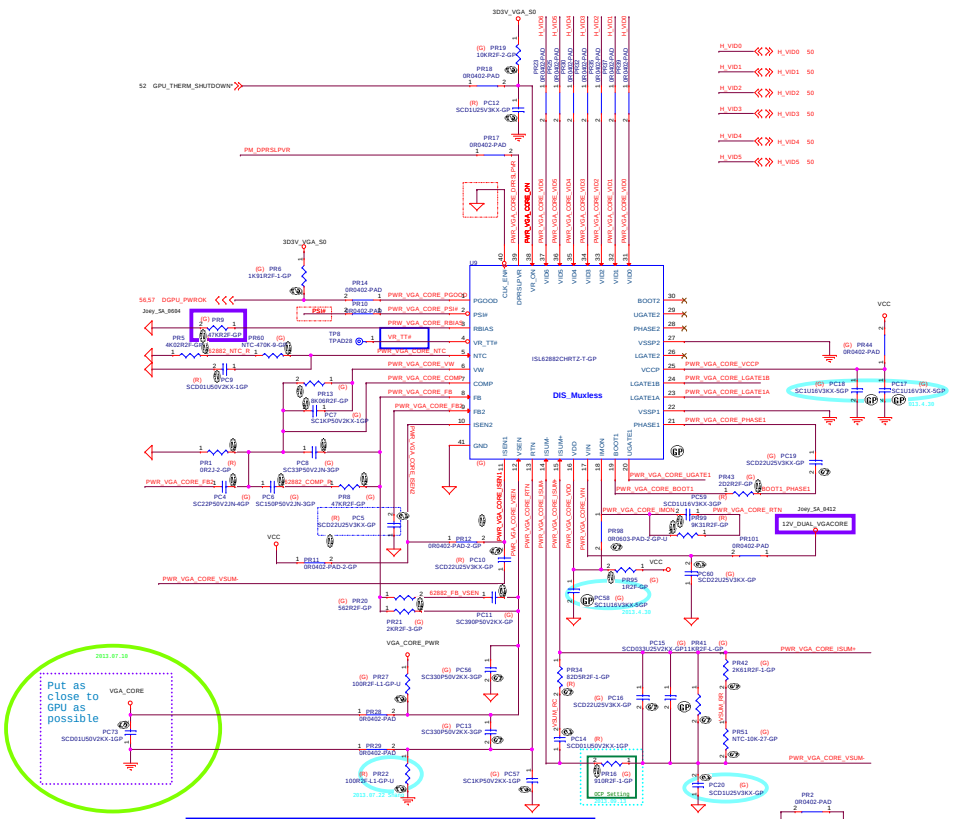
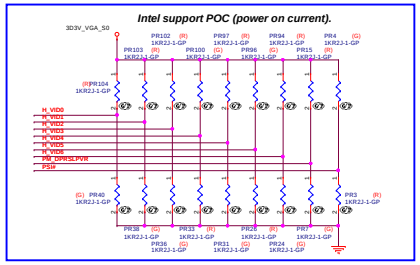
Title: GPU_DDR3 64MX16

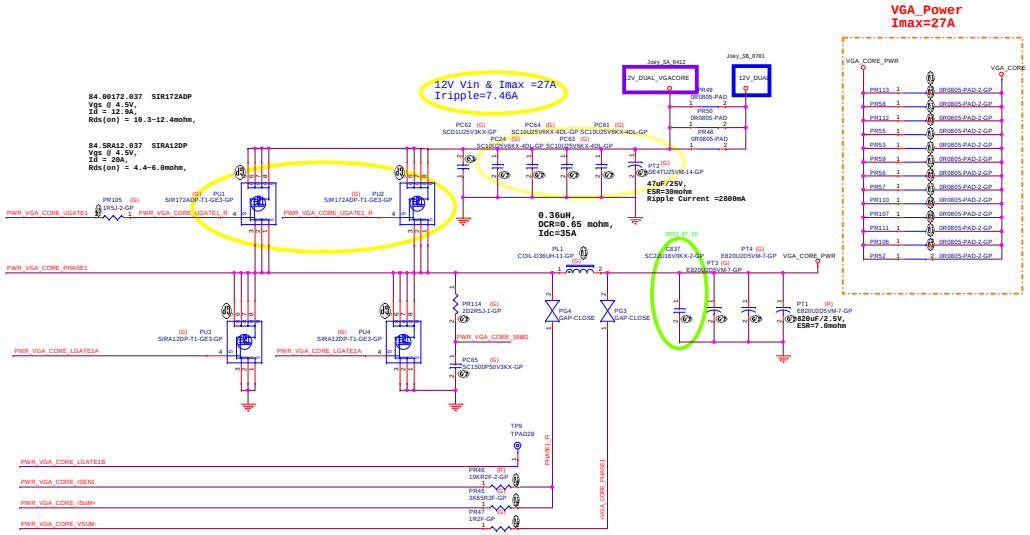
| Size | Document Number | Rev |
|---|---|---|
| D | Rosa_Tigris AIO | 1 |

Date: Monday, January 06, 2014 Sheet 54 of 58

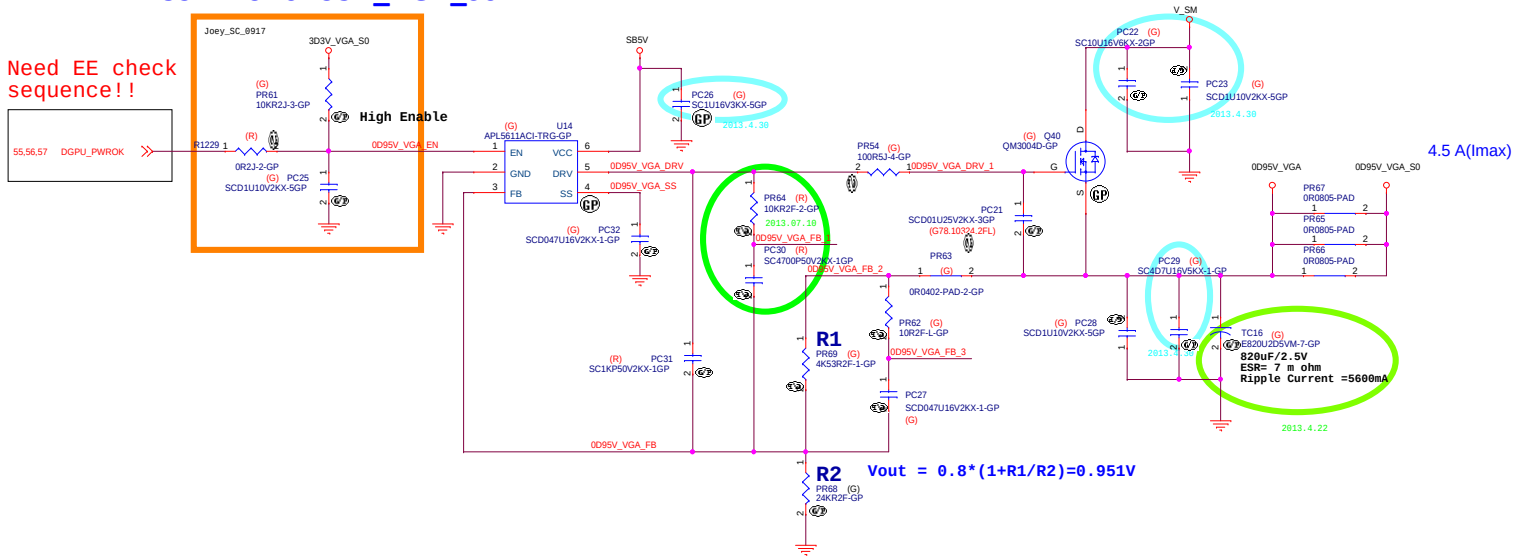


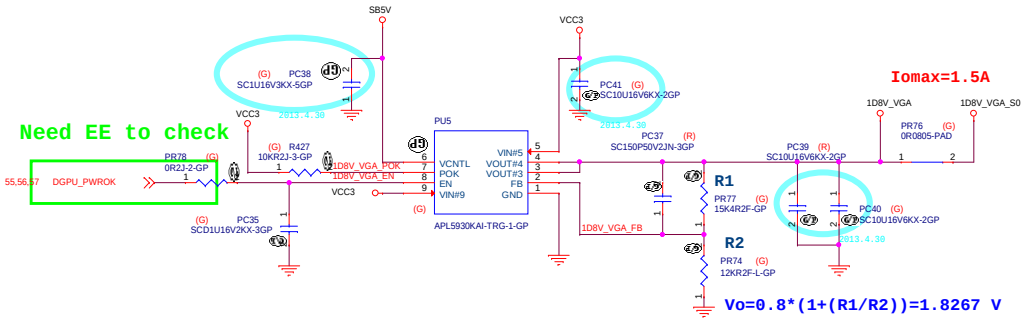

| VGA Vcore 1.0V | | | | | | |
|---|---|---|---|---|---|---|
| VID0 | VID1 | VID2 | VID3 | VID4 | VID5 | VID6 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |



# APL5912 for 0D95V_VGA_S0




# APL5930 for 1D8V_VGA_S0




<Variant Name>

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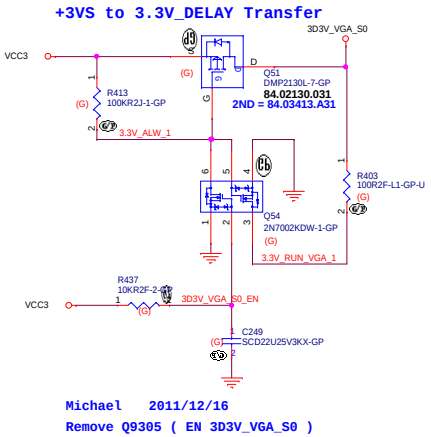
Hsichih, Taipei

Title: GPU_POWER 0D95V/1D8V

Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

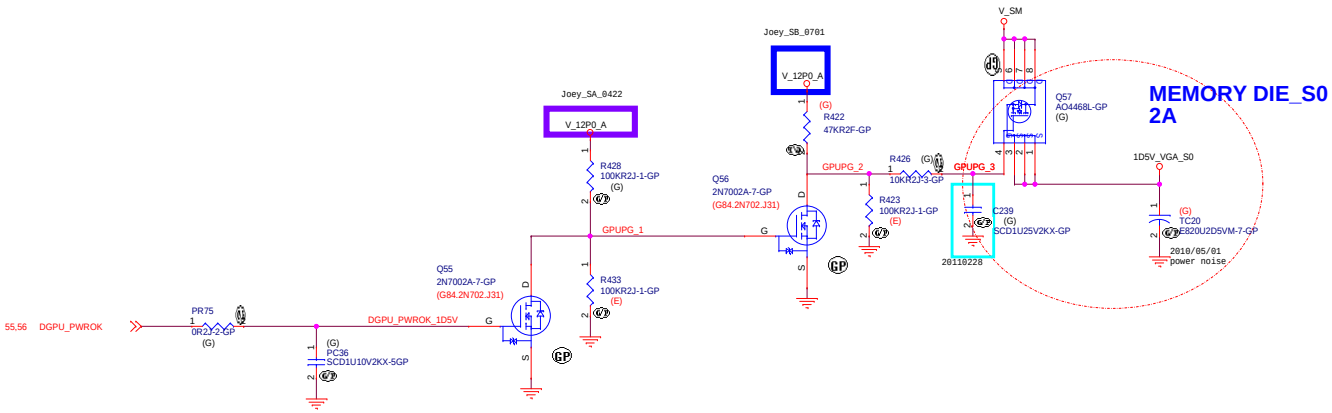
Date: Monday, January 06, 2014 | Sheet 56 of 58

## 3D3V_VGA_S0




## 1D5V_VGA_S0

20110103
GPU VCORE -> MEMORY POWER

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Title: GPU_POWER 3D3V/ 1D5V

Size: C | Document Number: Rosa_Tigris AIO | Rev: 1

Date: Monday, January 06, 2014 | Sheet 57 of 58

# Change list

| Change Number | DATE | Change | | Page | Reason | comment |
|---|---|---|---|---|---|---|
| 1001 | 2013/12/24 | Remove SPR1 | A00 | 33 | ME request | Joey |
| | | Remove INTRU1 | A00 | 18 | Customer request | Joey |

# Stack up

## 6-1.2-7a(2.40) stack up and impedance

| | | | |
|---|---|---|---|
| 疊構編號 | 6-1.2-7a | 注意事項 | 1. Impedance Control tolerance +/- 10% |
| 完成板厚 ( mm ) | 1.2 ± 0.12 | | 2. Coupon 製作方式及 Impedance report 請依照Wistron規範製作 |

**Stack up**

| | | | Thickness (mil) |
|---|---|---|---|
| L1 | TOP | [redacted] | 1.7 |
| | | PP | 2.7 |
| L2 | G/P ※3 | [redacted] | 1.2 |
| | | Core | 4 |
| L3 | Signal | [redacted] | 1.2 |
| | | PP | 24 |
| L4 | Signal | [redacted] | 1.2 |
| | | Core | 4 |
| L5 | G/P | [redacted] | 1.2 |
| | | PP | 2.7 |
| L6 | Bottom | [redacted] | 1.7 |
| | | Total | 45.6 |

**Impedance Request List**

| Spec \ Layer | L1 (Ref. Plane) ※1 | L3 (Ref. Plane) | L4 (Ref. Plane) | L6 (Ref. Plane) |
|---|---|---|---|---|
| **Single Ended Type (Trace width : mil)** | | | | |
| 27.4Ω | 12.0 (L2) | 16.0 (L2/L5) | 16.0 (L2/L5) | 12.0 (L5) |
| 33Ω | 9.0 (L2) | 12.0 (L2/L5) | 12.0 (L2/L5) | 9.0 (L5) |
| 34Ω | 8.5 (L2) | 11.5(L2/L5) | 11.5 (L2/L5) | 8.5 (L5) |
| 35Ω | 8.0 (L2) | 10.5 (L2/5) | 10.5 (L2/5) | 8.0 (L5) |
| 37.5Ω | 7.0 (L2) | 9.5 (L2/L5) | 9.5 (L2/L5) | 7.0 (L5) |
| 39Ω | 6.5 (L2)※4 | 9.0(L2/L5) | 9.0(L2/L5) | 6.5 (L5)※4 |
| 40Ω | 6.5 (L2)※4 | 8.5 (L2/L5) | 8.5 (L2/L5) | 6.5 (L5)※4 |
| 42Ω | 5.5 (L2) | 7.5 (L2/L5) | 7.5 (L2/L5) | 5.5 (L5) |
| 45Ω | 5.0 (L2) | 6.5 (L2/L5) | 6.5 (L2/L5) | 5.0 (L5) |
| 48Ω | 4.5 (L2) | 5.5 (L2/L5) | 5.5 (L2/L5) | 4.5 (L5) |
| 50Ω | 4.0 (L2) | 5.0 (L2/L5) | 5.0 (L2/L5) | 4.0 (L5) |
| 52Ω | 3.5 (L2) ※2 | 4.5 (L2/L5) | 4.5 (L2/L5) | 3.5 (L5) ※2 |
| 55Ω | NA | 4.0 (L2/L5) | 4.0 (L2/L5) | NA |
| **Differential Type (Trace width/Space width/Trace width: mil)** | | | | |
| 110Ω | NA | 3.5/13/3.5(L2/L5) | 3.5/13/3.5(L2/L5) | NA |
| 100Ω | 3.5/10/3.5(L2) | 4/9/4(L2/L5) | 4/9/4(L2/L5) | 3.5/10/3.5(L5) |
| 95Ω | 3.5/6/3.5(L2);4/10/4(L2) | 4/6.5/4(L2/L5) | 4/6.5/4(L2/L5) | 3.5/6/3.5(L5);4/10/4(L5) |
| 93Ω | 3.5/5.5/3.5(L2);4/8/4(L2) | 4/5.5/4(L2/L5);5/9/5(L2/L5) | 4/5.5/4(L2/L5);5/9/5(L2/L5) | 3.5/5.5/3.5(L5);4/8/4(L5) |
| 90Ω | 4/6/4(L2) | 4/5/4(L2/L5); 5/8/5(L2/L5) | 4/5/4(L2/L5); 5/8/5(L2/L5) | 4/6/4(L5) |
| 85Ω | 4/4.5/4(L2);5/8/5(L2) | 5/5.5/5(L2/L5) | 5/5.5/5(L2/L5) | 4/4.5/4(L5);5/8/5(L5) |
| 80Ω | 5/5/5(L2) | 6/6/6(L2/L5) | 6/6/6(L2/L5) | 5/5/5(L5) |
| 75Ω | 6/6/6(L2) | 7/6/7(L2/L5) | 7/6/7(L2/L5) | 6/6/6(L5) |
| 72Ω | 7/8/7(L2) | 7/5/7(L2/L5) | 7/5/7(L2/L5) | 7/8/7(L5) |
| 70Ω | 7/6/7(L2) | 8/6/8(L2/L5) | 8/6/8(L2/L5) | 7/6/7(L5) |
| 68Ω | 6.5/4/6.5(L2) | 7.5/4/7.5(L2/L5) | 7.5/4/7.5(L2/L5) | 6.5/4/6.5(L5) |
| 65Ω | 8/6/8(L2) | 9/5/9(L2/L5) | 9/5/9(L2/L5) | 8/6/8(L5) |

**Remark:**

※ 1: "Ref. Plane" means the reference plane of the traces.
※ 2: Trace space should be wider than 4.5mil.
※ 3: G is GND, P is PWR
※ 4: Only choose one signal to control on layer L1&L8